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BERTS-325C

BIT ERROR MEASUREMENT SYSTEM

SYSTEMS MANUAL

FORM 0225-0983E
PART NO. 8200-0009

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A UNIT OF
GENERAL SIGNAL

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TAU-TRON INC, 10 LYBERTY WAY, WESTFORD, MA 01866, (508) 692-5100
1-800-TAU-TRON (1-800-828-8766)—FAX (508) 692-1938—TELEX 750245

– WARRANTY –

ALL TAU-TRON TEST SETS ARE WARRANTED AGAINST ANY DEFECTS IN MATERIAL AND WORKMANSHIP, FOR A PERIOD OF *3 YEARS.*

This Warranty applies from the date of delivery for all Tau-tron test sets. Other manufacturers products offered by Tau-tron such as printers, cables, etc. are covered to the extent of their own warranty. Calibration of Tau-tron test sets is covered for 1 year from date of delivery. However, some restrictions apply; see your salesman for further details.

We will repair or replace test sets which, upon our examination, prove to be defective during the warranty period, except in cases of product abuse or attempted field repair.

No other Warranty, expressed or implied, including fitness for purpose, merchantability or otherwise, is given.

For assistance, contact Customer Service with details of the instrument model, serial numbers, and malfunction; see Repair Returns below.

SHIPPING DAMAGE

If any signs of damage are noticed on the outside of the carton, make a request for the carrier's agent to be present during unpacking. If external damage is found on the instrument, follow Repair Returns procedure below.

Check the electrical performance of the instrument as soon as possible after receipt. If there are any malfunctions, follow Repair Returns procedure below.

REPAIR RETURNS

For mechanical damage or electrical malfunctions, notify Tau-tron immediately. If the damage occurred during shipping, also notify the carrier. To return a unit for repair:

1. Call the Customer Service Department, **(508) 692-5100** (800-TAU-TRON [800-828-8766], outside MA), for a **Repair Authorization Number**. The use of this number reduces administrative delays and ensures the prompt return of your unit.
2. Complete and **attach the Repair Tag**, located in the back of the manual, **to your unit** for positive identification.
3. Pack the unit in the original shipping carton and packing materials, if available. Otherwise use a double-walled carton (test strength of 350 lb; 159 kg) and shock-absorbing material such as bubblewrap, to prevent the unit from moving in the carton during transit. Secure the carton by sealing with heavy paper tape.
4. Send to: Tau-tron Inc.
   10 Lyberty Way
   Westford, MA 01886
   Attn: Customer Service

PREFACE

Sophisticated instrumentation systems with GPIB now require performance capability beyond that obtainable with instruments that do not have GPIB. This, as a result, has created a need for test instrumentation users to be more adept in the use of GPIB compatible test instruments. Similarly, it has become necessary for instrumentation manufacturers to provide professionally-written and designed documentation.

This manual is the result of such a pain-staking endeavor and is designed primarily to explain the operational features of the BERTS-325C/650 Bit Error Measurement System and its associated GPIB. In the manual, two appendices are presented to assist the user in becoming more familiar with the system's GPIB operation. The first appendix briefly describes the software Version 4 Interface Card implemented in the MF-5 Mainframe of the BERTS-325C/650. The second appendix summarizes the BERTS-325C/650 GPIB operation and presents a consolidated guide or "ready reference" that describes the GPIB operation of each module incorporated in the BERTS-325C/650.

The primary purpose of the ready reference guide is to give the user, who is familiar with IEEE-488 GPIB operation, instant access to the BERTS-325C/650 GPIB modes of operation, message format, and measurement output. However, for those users who are unfamiliar with the system's GPIB operation, reference to the respective sections describing each module's GPIB operation should be addressed first.

CONTENTS PAGE

1. BERTS-325C BIT ERROR MEASUREMENT SYSTEM

1.1 Scope 1-1
1.2 Description 1-2
1.3 Specifications 1-3

1.3.1 Input Power Requirements 1-4

1.4 Back-To-Back Performance Check 1-5

1.4.1 Purpose 1-5
1.4.2 References 1-5
1.4.3 Connections 1-5
1.4.4 Control Settings 1-5
1.4.5 Procedure 1-6

1.4.5.1 Receiver Synchronization 1-6
1.4.5.2 Reference Data Tracking 1-6
1.4.5.3 16-Bit Word 1-7

1.4.6 Synchronization vs. Frequency Check 1-7
1.4.7 MB-302 Frequency Mode Check 1-7
1.4.8 Auto-Ranging Bit Error Rate 1-7

1.4.8.1 Auto-Ranging with Internal Error Inject 1-7

1.5 System Under Test Connections 1-8

1.5.1 Typical Test Setup 1-8
1.5.2 Receiver Synchronization 1-8

2. MF-5 MAINFRAME

2.1 Description 2-1
2.2 Specifications 2-2

2.2.1 Options 2-2

2.3 Input Power Connections 2-3

2.3.1 Site Requirements 2-3

2.4 Cooling 2-4
2.5 Module Insertion/Removal 2-5

2.5.1 Module Lock 2-5
2.5.2 Inserting Modules 2-5
2.5.3 User Built Modules 2-5
2.5.4 MF-5 Mainframe Rackmounting 2-6

2.6 Operation 2-7
2.7 Theory of Operation 2-8

2.7.1 AC Input 2-8
2.7.2 DC Output 2-8

2.8 Service 2-9

2.8.1 Routine Service 2-9
2.8.2 Repair Returns 2-9
2.8.3 Assistance 2-9
2.8.4 Trouble Analysis 2-9
2.8.5 Output Characteristics 2-10
2.8.6 Module Loads 2-10
2.8.7 Test Procedure 2-10
2.8.8 GPIB 2-11

3. MS-302 CLOCK SOURCE

3.1 Description 3-1
3.2 Specifications 3-2
3.3 Installation 3-3
3.4 Front Panel 3-4
3.5 Operation 3-6

3.5.1 Output Level Setting 3-6
3.5.2 Continuous Frequency Select 3-6
3.5.3 Crystal Frequency Select 3-7

3.6 Theory of Operation 3-8

3.6.1 Clock Source Board 3-8
3.6.2 Front-Panel Display Board 3-8
3.6.3 Module Power Supplies 3-9

3.7 GPIB Option 3-10
3.8 Service 3-11

3.8.1 Routine Service 3-11
3.8.2 Repair Returns 3-11
3.8.3 Assistance 3-12
3.8.4 Trouble Analysis 3-12

4. MN-302 BERT TRANSMITTER

4.1 Description 4-1
4.2 Specifications 4-2
4.3 Installation 4-4
4.4 Front Panel 4-5
4.5 Operation 4-7

4.5.1 Output Level Select 4-7
4.5.2 Clock Input Connection 4-7
4.5.3 Pattern Selection 4-7

4.5.3.1 Pattern Select Indicators 4-8

4.5.4 Error Inject 4-8
4.5.5 System Under Test Connection 4-8
4.5.6 Oscilloscope Use 4-9

4.6 Theory of Operation 4-10

4.6.1 Input Clock Amplifier and Clock Distribution 4-10
4.6.2 Pattern Generator 4-10

4.6.2.1 Frame Sync Counter and All Zeros Detector 4-10
4.6.2.2 Fixed Word Pattern 4-11

4.6.3 Control Functions 4-12

4.6.3.1 Error Inject 4-12
4.6.3.2 NRZ/RZ 4-13
4.6.3.3 Data/Data 4-13
4.6.3.4 Data Inhibit 4-13

4.6.4 Output Amplifiers 4-13
4.6.5 Module Power Supplies 4-13

4.7 GPIB Option 4-14
4.8 Service 4-15

4.8.1 Routine Service 4-15
4.8.2 Repair Returns 4-15
4.8.3 Assistance 4-16
4.8.4 Trouble Analysis 4-16

5. MB-302 BERT RECEIVER

5.1 Description 5-1
5.2 Specifications 5-2
5.3 Installation 5-4
5.4 Front Panel 5-5
5.5 Operation 5-9

5.5.1 System Under Test Connection 5-9
5.5.2 Input Level Select 5-9
5.5.3 Reference Data Synchronization Modes 5-9

5.5.3.1 Auto 5-9
5.5.3.2 Manual Ref Data Select/Manual Sync 5-9
5.5.3.3 Manual Ref Data Select/EXT Command 5-10
5.5.3.4 Manual Ref Data Select/Burst Mode 5-10
5.5.3.5 External Ref Data 5-11

5.5.4 Counter Modes 5-13
5.5.5 Display Time 5-14
5.5.6 Printer Interface 5-15

5.6 Theory of Operation 5-16

5.6.1 Front-Panel Board 5-16

5.6.1.1 Input Clock and Data Amplifiers 5-16
5.6.1.2 6-Digit Display 5-16
5.6.1.3 Status, Ref Data, and other Indicators 5-17

5.6.2 Code ReSync Board 5-17

5.6.2.1 Clock Distribution 5-17
5.6.2.2 Reference Pattern Generator 5-17
5.6.2.3 Input Data Latch and Demultiplexer 5-17
5.6.2.4 Error Detector 5-18
5.6.2.5 Error Sampler 5-18
5.6.2.6 Frame Sync Counter 5-18
5.6.2.7 All Zero Detect 5-18
5.6.2.8 High-Speed Error Counter 5-19

5.6.3 Counter Board 5-19

5.6.3.1 Error Threshold 5-19
5.6.3.2 Time Base Control and Counter 5-20
5.6.3.3 Error Counter 5-20
5.6.3.4 Display time 5-20

5.6.4 The Synchronization Process 5-20

5.6.4.1 Auto Sync Mode 5-21
5.6.4.2 Manual Sync Modes 5-21

5.6.5 The Counting Process 5-21

5.6.5.1 Bit Error Rate Auto 5-21
5.6.5.2 Bit Error Rate Manual 5-22
5.6.5.3 Totalize 5-22
5.6.5.4 Frequency 5-22

5.6.6 BCD Interface 5-23
5.6.7 Module Power Supplies 5-23

5.7 GPIB Option 5-24
5.8 Service 5-29

5.8.1 Routine Service 5-29
5.8.2 Repair Returns 5-30
5.8.3 Assistance 5-30
5.8.4 Trouble Analysis 5-30

6. GPIB OPERATION

6.1 Description 6-1
6.2 MF-5 Mainframe Front Panel (GPIB) 6-3
6.3 MF-5 Mainframe Rear Panel (GPIB) 6-4
6.4 BERTS-325C GPIB capabilities 6-6

6.4.1 Response to GPIB Commands 6-6

6.5 Module I. D. 6-8

6.5.1 Specific Modules 6-8

7. PARTS

7.1 Replaceable Parts 7-1

8. DIAGRAMS

8.1 General 8-1

APPENDIX A- VERSION 4.0 IFC A-1

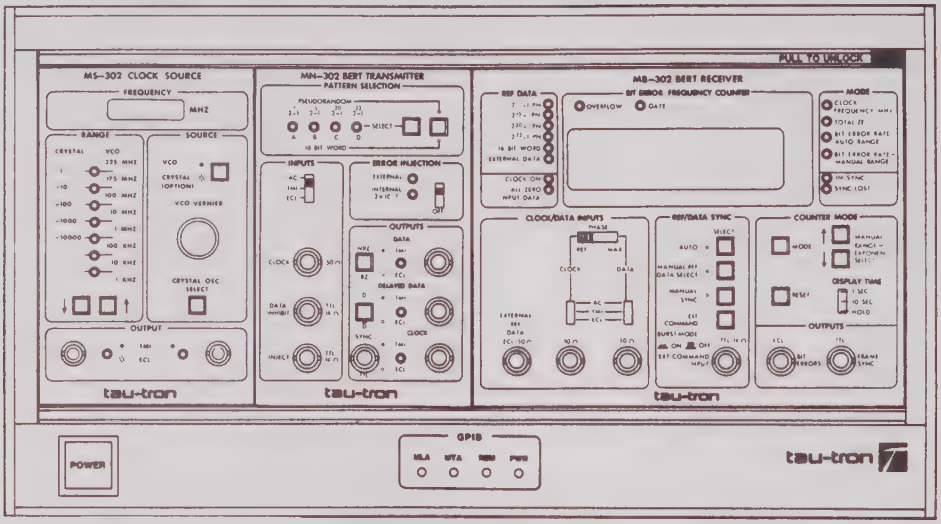
APPENDIX B- BERTS-325C/650 GPIB AND READY REFERENCE GUIDE B-1

1. BERTS-325C BIT ERROR RATE MEASUREMENT SYSTEM

1.1 SCOPE

This manual provides operation, testing applications, interfacing, and theory of operation for the BERTS-325C Bit Error Rate Measurement System.

1.2 DESCRIPTION



The Tau-Tron BERTS-325C Bit Error Rate Measurement System is a complete modular test set for bit error-rate measurements up to 325MHz. It generates both pseudorandom and fixed 16-bit patterns for stimulating the system under test and measures the bit-by-bit errors on the patterns as they are received from the system under test. Bit error-rate or total errors can be measured on continuous data, or on burst data for such applications as TDMA testing. Data and delayed-data outputs are included to facilitate QPSK test applications and a printer output is standard for automatic data logging.

The set consists of an MF-5 Mainframe, an MS-302 Clock Source, an MN-302 BERT Transmitter and an MB-302 BERT Receiver.

1.3 SPECIFICATIONS

Detailed specifications are given for each module in their respective sections.

System Clock Output	1kHz to 325MHz continuously variable. Output signal level can be set to 1V into 50 ohms to ground termination or ECL levels with a 50 ohms to -2V termination.
Data Output	1kb/s to 325Mb/s continuously variable, NRZ or RZ data format can be selected. Output signal level can be set to either 1V into 50 ohms to ground or ECL, terminated with 50 ohms to -2 volts.
Delayed Data Output	Same data rate and output signal levels as the data output. Data format is fixed as NRZ but the signal may be inverted by a front-panel pushbutton. The delay is 8 bits when referenced to the data output.
Clock Input	1kHz to 325MHz from the system under test. The input impedance may be set to AC coupled 50 ohms, DC coupled 50 ohms to ground or ECL 50 ohms to -2 volts. The amplitude must be 1V in the AC and DC coupled modes and 800mV to 1V in the ECL mode.
Data Input	1kb/s to 325Mb/s from the system under test. The input impedance may be set to AC coupled 50 ohms, DC coupled 50 ohms to ground or ECL 50 ohms to -2V. The data format should be NRZ and the amplitude in the range of 800mV to 1V.
Data Patterns	Pseudorandom or fixed word, as selected by front-panel pushbuttons with LED indicators. PSEUDORANDOM: 2^7-1 (127), 2^{15}-1 (32,767), 2^{20}-1 (1,048,575) or 2^{23}-1 (8,388,607) bits. FIXED WORDS: 16-bit, A: Alternating 1-0; B, C, and D: Random.
Synchronization	Four modes are available as selected by front-panel control: AUTOMATIC: Syncs automatically on proper pseudorandom code length or fixed-word. MANUAL: Sync triggered by front-panel pushbutton. EXTERNAL: Same as manual except sync attempt is initiated by a signal applied to the External Command Input. EXTERNAL REFERENCE DATA: A signal applied is used for comparison; sync acquisition is undefined.

MEASUREMENTS	Four modes are available, as selected by front-panel pushbuttons: TOTALIZE: Bit errors accumulated indefinitely. TIME RATE AUTO: Bit error-rate measured with automatic range selection of 10^{-2} to 10^{-9}, 3 digits plus 1-digit exponent. TIME RATE MANUAL: Bit error-rate measured with manual range selection of 10^{-2} to 10^{-9}, 3 digits plus 1-digit exponent. CLOCK FREQUENCY: Measures input clock frequency in MHz with 1kHz resolution, 6 digits.
Frame Sync	A TTL pulse from the transmitter can be used to trigger an oscilloscope. The period of this pulse is determined by the selected pattern. The receiver also generates a Frame Sync signal but is valid only when the receiver is synchronized to the incoming data.
Error Output	An RZ error pulse designed to drive an ECL termination is available at the front panel. The width of this signal is one half of the bit period at the selected operating data rate.
Display	6-digit display plus overflow.

1.3.1 INPUT POWER REQUIREMENTS

120, 220 or 240VAC ±10%, 48 to 66Hz, 240VA, via a 6-foot detachable power cord that connects to a rear-panel receptacle on the mainframe. Confirm that the proper AC input voltage range has been selected, see Section 2.3, Input Power connections for details.

Temperature	32 to 95°F (0 to 35°C).
Humidity	0 to 95% RH max at 20°C, non-condensing.
Mechanical	DIMENSIONS: 10 in. high x 17.75 in. wide x 18.5 in. deep. WEIGHT: 47 lb net, 54 lb shipping.

1.4 BACK-TO-BACK PERFORMANCE CHECK

1.4.1 PURPOSE

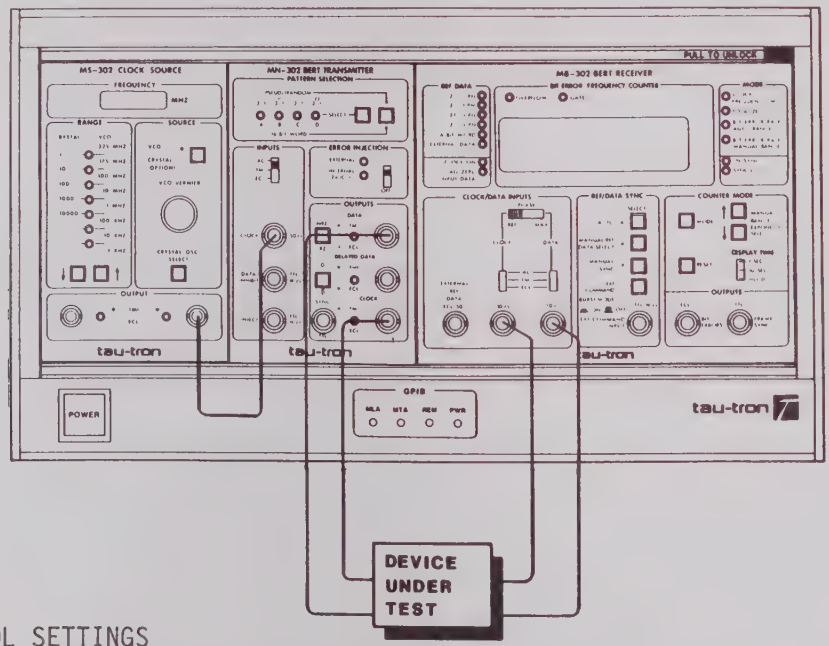
The purpose of this check is to acquaint the operator with the various controls of the BERTS-325C and to provide a means of verifying proper system operation before connection is made to some device or system under test.

1.4.2 REFERENCES

Please refer to the individual module sections for a detailed description of the controls and the operating instructions.

1.4.3 CONNECTIONS

Make the connections as shown in the following diagram. The impedance of the interconnecting cables must be 50 ohms, the length may be any convenient length which will still allow unobstructed access to the front-panel controls.



1.4.4 CONTROL SETTINGS

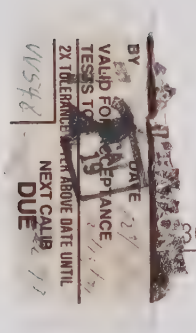
Set the individual module controls to the settings as described in the following instructions. In some cases the setting must be made internally on the module circuit board; the appropriate module section should be referenced in order to make the proper internal settings.

MS-302 CLOCK SOURCE

SOURCE.....VCO
RANGE.....10-100MHz
VCO VERNIER.....50MHz (read on the FREQUENCY display)
OUTPUT.....TMI (internal switch)

MN-302 BERT TRANSMITTER

INPUT (CLOCK).....TMI
PATTERN SELECT.....PSEUDORANDOM 2^7-1
ERROR INJECT.....OFF
DATA OUTPUT.....TMI (internal switch)
DELAYED DATA OUTPUT..TMI (internal switch)
CLOCK OUTPUT.....TMI (internal switch)
DATA NRZ/RZ.....NRZ
DELAYED DATA D/$\bar{D}$.....D



302 BERT RECEIVER

CLOCK INPUT.....TMI
DATA INPUT.....TMI
REF/DATA SYNC.....AUTO
COUNTER MODE.....TOTALIZE
DISPLAY TIME.....1 SEC.

1.4.5 PROCEDURE

1.4.5.1 RECEIVER SYNCHRONIZATION

The MB-302 CLOCK ON LED should be ON and the ALL ZERO INPUT DATA LED should be OFF indicating that clock and data signals are being received from the MN-302. Observe the error display on the MB-302, if the display is constantly changing, then the receiver may not be synchronized. Select a different position on the CLOCK/DATA PHASE switch. A position should be reached where the error display freezes to a fixed totalized value. The IN SYNC, SYNC LOST and OVERFLOW LEDs should be ON; push the RESET button, the SYNC LOST and OVERFLOW LEDs should be OFF.

1.4.5.2 REFERENCE DATA TRACKING

Push the PSEUDORANDOM PATTERN SELECT button on the MN-302, the REF DATA LED should track the selection from the MN-302 and the error display should show a fixed TOTALIZE value after automatic synchronization at each pattern. Reset the counter after each synchronization.

1.4.5.3 16-BIT WORD

Select 16-BIT WORD on the MN-302, the 16-BIT WORD pushbutton will latch on and words A, B, C, or D will be transmitted. To change the word, push the SELECT button. The MB-302 REF DATA should show the 16-BIT WORD as the received pattern, the IN SYNC and SYNC LOST LEDs will be ON, the OVERFLOW may be ON; pushing the COUNTER MODE RESET should clear the OVERFLOW and SYNC LOST LEDs.

1.4.6 SYNCHRONIZATION VS. FREQUENCY CHECK

Return the MN-302 to PSEUDORANDOM, 2^7-1 PATTERN SELECT. Select the next test frequency on the MS-302, this can be done by the combination of the RANGE SELECTION and the VCO VERNIER setting.

Observe the MB-302 error display; if it begins to show errors as the frequency is changed or show errors at the desired test frequency, readjust the CLOCK/DATA PHASE switch. A position on the switch will be reached where the TOTALIZE errors become fixed and will reset to zero when the RESET pushbutton is pushed.

NOTE: At the higher frequencies, in the range of 275 to 325MHz, a more frequent adjustment of the PHASE switch may be required as the freqency is varied.

1.4.7 MB-302 FREQUENCY MODE CHECK

Set the COUNTER MODE to CLOCK FREQ by use of the MODE pushbutton. The display will show the frequency as a six-digit number in MHz and resolution to 1kHz. This number should agree within the range of the least significant digit of the frequency displayed on the MS-302.

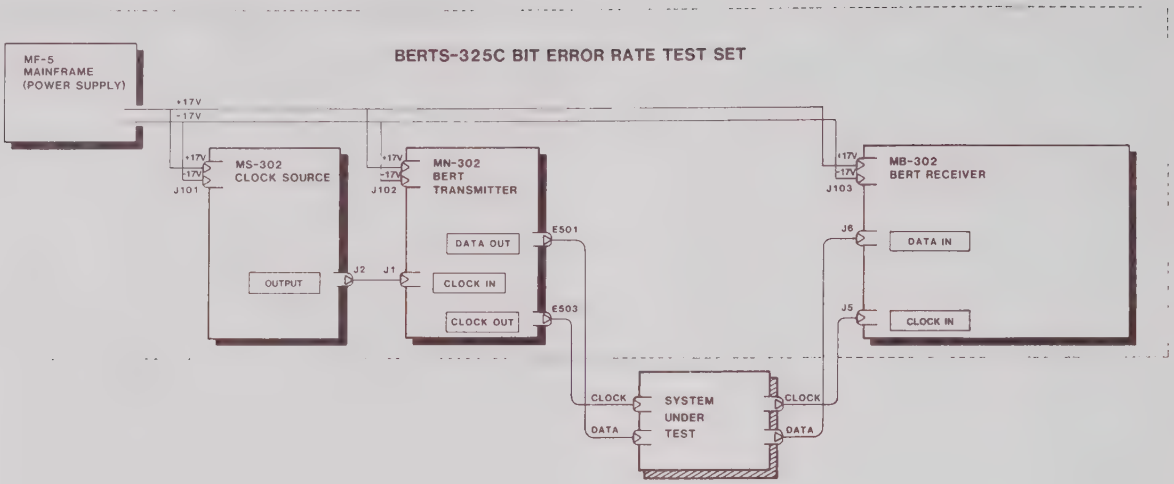
1.4.8 AUTO-RANGING BIT ERROR RATE

Set the COUNTER MODE to BIT ERROR RATE-AUTO RANGING, the display should show all zero errors as a three-digit number plus a single-digit exponent. The exponent will start at the highest error-rate (10^{-2}) and automatically scale down toward the lowest error-rate (10^{-9}).

1.4.8.1 AUTO-RANGING WITH INTERNAL ERROR INJECT

Set the MN-302 ERROR INJECT to INTERNAL, the MB-302 should display 2.00×10^{-2} within ±1 count.

1.5 SYSTEM UNDER TEST CONNECTIONS



1.5.1 TYPICAL TEST SETUP

NOTE: The inputs and outputs of the unit under test must be compatible with the BERTS-325C. The MN-302 CLOCK and DATA outputs must drive a DC load which is either 50 ohms to ground (TMI) or 50 ohms to -2 volts (ECL). The MS-302 must also drive a similar DC load; and when driving other TMI modules, the output of the MS-302 must agree with the input of the module. The same caution must be observed when connecting the MB-302 receiver to the unit under test; the input circuit setting must agree with the driving circuit.

Failure to observe these rules will result in waveform distortion which may cause incorrect system operation.

1. Set the clock to the desired test frequency.

1.5.2 RECEIVER SYNCHRONIZATION

1. Check that the MB-302 CLOCK ON LED is lit and the ALL ZERO INPUT DATA LED is out.
2. Set the REF DATA/SYNC to AUTO.
3. Observe the error counter display in the TIME RATE AUTO MODE, adjust the CLOCK/DATA PHASE switch for minimum error-rate.

4. Check that the MB-302 REF DATA agrees with the data pattern on the MN-302.
   The IN SYNC LED should be ON.
   The SYNC LOST LED should be ON.
   The OVERFLOW LED may be ON if this is an initial test start-up.

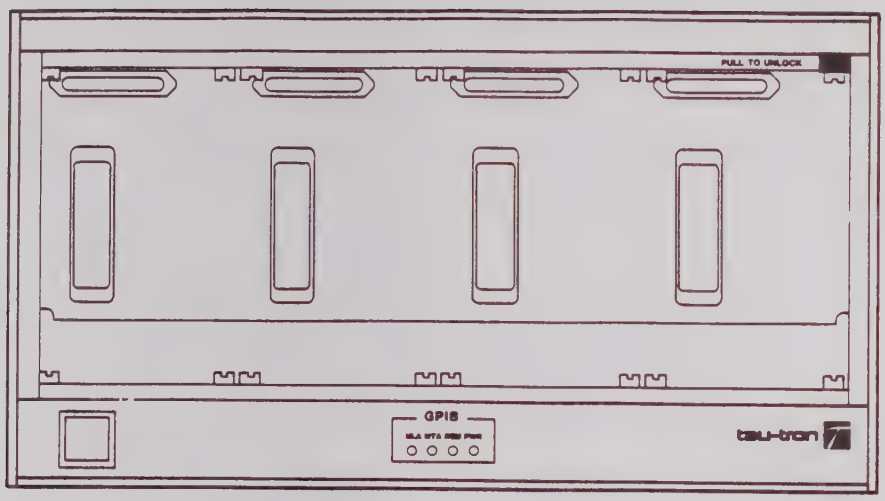
5. Push the COUNTER MODE RESET button, the SYNC LOST and OVERFLOW LEDs should go out.

If the IN SYNC LED does not come on or the REF DATA LEDs are not stable, then re-check the input data or readjust the CLOCK/DATA PHASE switch.

If the REF DATA LED does not agree with the MN-302 PATTERN SELECT LED, (especially if the MN-302 is in PSEUDORANDOM and the MB-302 indicates a 16-BIT WORD) then the ALL ZEROS INPUT DATA LED should be ON, indicating that digital data are not reaching the MB-302. Recheck all connections and transmitter patterns, take proper corrective action and try synchronization again.

2. MF-5 MAINFRAME

2.1 DESCRIPTION



The Tau-Tron MF-5 Mainframe provides power, cooling, and mechanical support for TMI® (Tau-Tron Modular Instrumentation) plug-in modules.

2.2 SPECIFICATIONS

Modules	Accepts up to 4 quarter-size modules, 2 half-size modules, or 1 full-size module and supplies unregulated +34V, +17V, -34V, and -17V to all modules via internal wiring.
Cooling	Two rear-mounted fans exhaust air through the top.
Power	120V±10%, 220V±10% or 240V±10%, 48 to 66Hz AC, via a 6-foot detachable cord (supplied) that connects to a rear-panel receptacle.
Mechanical	Benchmount, blue-painted aluminum case with convenient carrying handles mounted on sides. Rack Panel adaptor kit available, see Option 05. DIMENSIONS: 10 in. high x 17.75 in. wide x 18.5 in. deep overall including rubber feet. WEIGHT: 38 lb net, 45 lb shipping.
Accessories Supplied	AC power cable and instruction manual.

2.2.1 OPTIONS

Option 02 IEEE-488 Interface	This option (GPIB) provides for remote control of up to four modules plugged into the MF-5 (four with Listen capability, one with Talk capability).
Option 05 Rack Panel Kit	This kit includes brackets to adapt the MF-5 front panel for mounting in a standard 19-in. rack. Panel height is 10.5 in. and depth behind panel is 17 in. The MF-5 requires additional support in the form of a shelf with side panels and/or rear base.
Accessories Available	EC-1 Cable to connect module to mainframe with module removed for servicing ease.

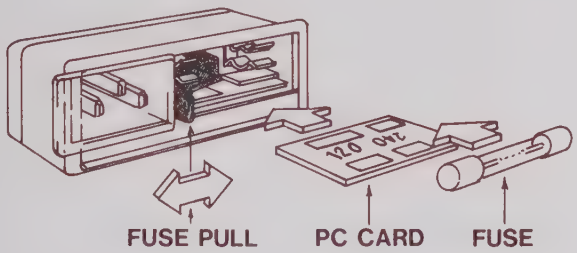
2.3 INPUT POWER CONNECTIONS

CAUTION: Be sure the unit is set for the proper line-voltage range before connecting to the AC line. If the incorrect range is selected, the unit could be damaged.

AC Power — Three-wire connector, accepts the power cord supplied. Before connection, check that the proper line-voltage range is selected and the proper fuse is installed (120VAC for 3A Slo-Blo and 220 or 240VAC for 1.5A Slo-Blo).

a. Slide cover door to the left and rotate FUSE PULL to the left.

b. Remove fuse and check for proper value.

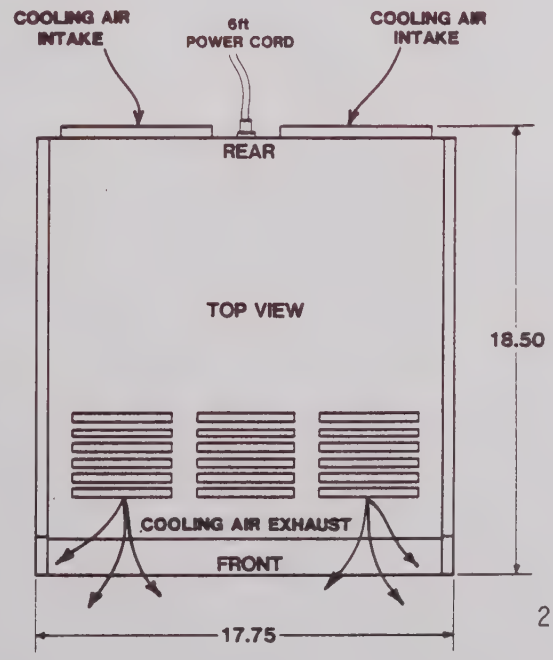


c. Check that the legend on the PC Card in the connector reads the proper line-voltage range. If it doesn't, remove the card (pull straight out), turn it around, and reinsert.

d. Rotate FUSE PULL to the right, back into its normal position and reinstall the fuse.

2.3.1 SITE REQUIREMENTS

AC Power	120, 220 or 240V ±10%, 48 to 66Hz AC.
Temperature	32 to 95°F (0 to 35°C) operating.
Humidity	0 to 95% RH max at 20°C, non-condensing.
Size	10 in. high x 17.75 in. wide x 18.5 in. deep.
Weight	38 lb net.
Clearances	2 in. min rear, 1/2 in. min top, to allow cooling air to be drawn in the rear and exhausted through the top.



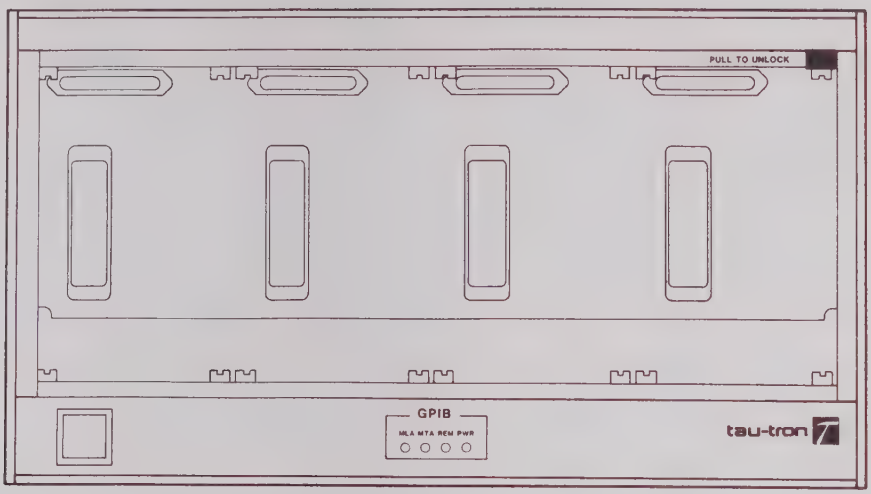
2.4 COOLING

The MF-5 contains twin cooling fans. Cooling air is drawn in through the rear panel, circulated through the modules, and exhausted through the top of the mainframe. To ensure good air flow for proper module cooling, all four module positions should be filled with functional modules or blank plug-ins.

The fan filters should be kept clean for adequate air flow. To clean, refer to Section 2.8.1, Routine Service.

CAUTION: The top cover of the MF-5 Mainframe should be placed on the mainframe with the the slotted end facing the front panel, otherwise proper circulation will not be realized.

2.5 MODULE INSERTION/REMOVAL



2.5.1 MODULE LOCK

The module lock-in bar holds all modules securely in the mainframe. The locking control lever is located at the upper right-hand corner of the front panel. When the lever is pushed in, all modules are locked in place; when the lever is pulled out, all modules are unlocked for removal.

2.5.2 INSERTING MODULES

With the module locking lever pulled out, the TMI modules will slide easily into place. Standard TMI modules will operate in any module position. However, some modules with rear-panel I/O functions, like standard printer output on the MB-302 are equipped with an auxiliary connector; this connector must be aligned with its counterpart in the mainframe. Mainframes equipped with Option 02, GPIB, have auxiliary connectors in all four positions.

Power is connected automatically as each module is pushed into place. The single power switch turns all the TMI modules on and off simultaneously. When the modules have been inserted, push the locking control lever in to lock all modules in the mainframe.

2.5.3 USER BUILT MODULES

The BP-2 and BP-4 blank modules, normally used to fill empty module positions, can also be used to house user built circuits. These blank modules are equipped with the standard TMI 24-pin power connectors supplying the unregulated ±17 and ±34 DC voltages. The total current drawn must not exceed 4A from the positive supply or 8A from the negative supply. See Section 2.7.2 for voltage pin assignments.

2.5.4 MF-5 MAINFRAME RACKMOUNTING (OP-05)

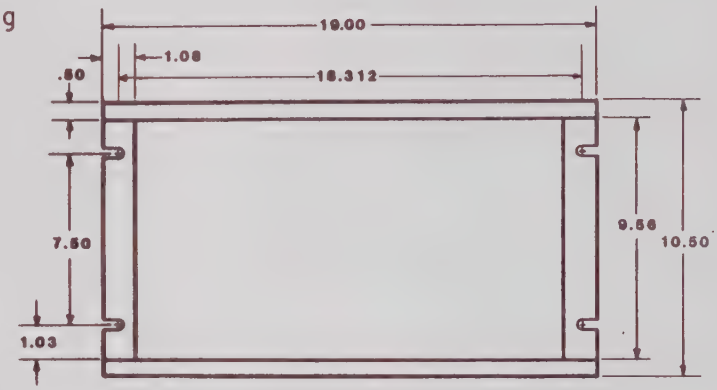
These instructions are to adapt the MF-5 for mounting in a standard 19-in. rack. They are for use with the OP-05 kit which includes the following parts:

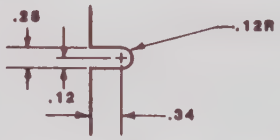
2 ea. Mounting bracket, Tau-Tron 9705-4317
2 ea. Filler bracket, Tau-Tron 9705-4316
4 ea. Screws, 6-32 X ½in. Phillips head
4 ea. Lockwashers, No. 6
4 ea. Spacers, .25 OD X .19 ID X .12 long

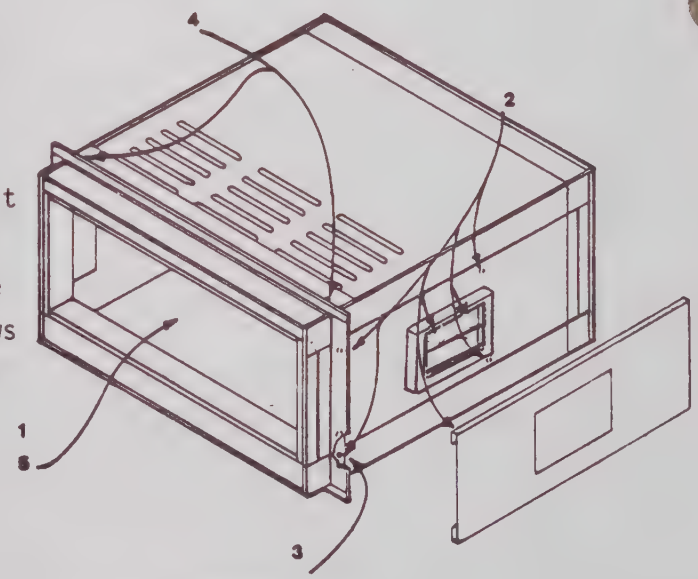
1. Module Removal — Remove the modules.

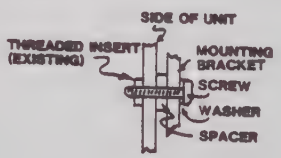
2. Side-Panel Removal — From the inside of the unit, remove the 4 Phillips-head screws that secure the side panel to the frame and remove both side panels. Remove both side-handle assemblies by removing both sets of inner washers and nuts. The screws and components may be set aside as they are not used for rackmounting.

3. Mounting — Attach each mounting bracket (supplied) to the sides of the unit using the hardware supplied. Fasten the screws into the existing threaded inserts in the frame.









4. Filler Brackets — Remove the 2 front screws from the top and bottom covers. Install the filler brackets (supplied) to the top and bottom of the unit and secure with the screws previously removed.

5. Module Insertion — Reinstall the modules.

NOTE: Ensure that some type of additonal support is provided. A shelf with side panels and/or rear support is recommended.

2.6 OPERATION

Once the system is connected to the AC line and the modules are installed, it is ready to operate.

Power on: Set the POWER switch in (on); the indicator in the switch should light. Power is now applied to all modules in the mainframe and they should be operational.

System interconnections and module operation are described in the instruction manuals for the individual modules.

Power off: Set the POWER switch out (off); the indicator in the switch should extinguish.

2.7 THEORY OF OPERATION

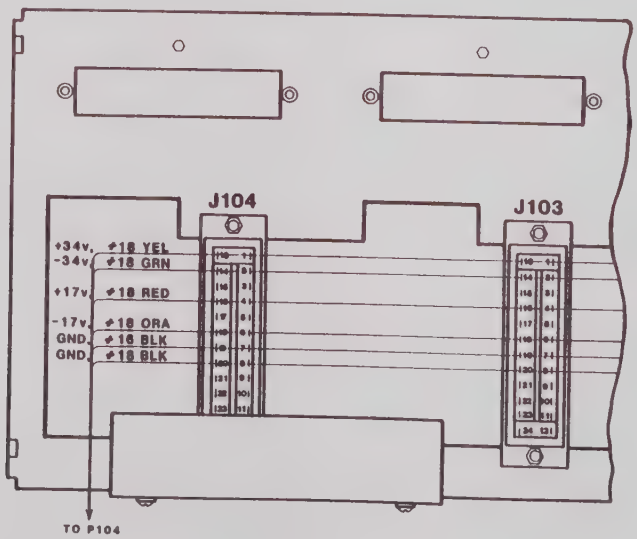
2.7.1 AC INPUT

The AC input is applied via a 6-foot detachable power cord to a rear-panel connector. The connector contains the AC input adjustments for various line voltage values. Adjusting these inputs selects different taps on the primary of the power supply transformer such that the transformer secondary voltages do not exceed safe recommended values. See Section 2.3 for the input voltage adjustments. The AC line fuse is also in this connector.

2.7.2 DC OUTPUT

The unregulated DC voltages required to power the modules are ±34V and ±17V. The power transformer includes two center-tapped secondary windings, each of which is connected to a full wave bridge rectifier. One rectifier develops the +34V unregulated supply while the other rectifier, in an identical but opposite polarity circuit, develops the -34V unregulated voltage. The +17 and -17 unregulated voltages are derived from the center taps of the transformer windings which drive the +34 and -34V diode bridges. Some filtering is provided by the mainframe, the +34, -34 and +17V supplies are smoothed by an 11,000 micro-farad electrolytic capacitor on each output; the -17V supply, which has the highest current requirement, is filtered by a 45,000 micro-farad capacitor.

All output voltages are bussed along the rear-panel connector which accepts the power connector input on the module rear panel. All power supply connectors are wired identically, as shown below.



2.8 SERVICE

2.8.1 ROUTINE SERVICE

Periodically clean the two rear-panel filters to maintain proper airflow for adequate cooling. The frequency of this maintenance will depend on the operating environment.

1. Insert a blade screwdriver into one of the notches located at each corner on the side of the filter holder and pry the holder off.
2. Use a vacuum cleaner to clean the filter, screen and cover.
3. Reinstall the filter and screen and secure by snapping the cover back on.

2.8.2 REPAIR RETURNS

For mechanical damage or electrical malfunctions, refer to Page ii, REPAIR RETURNS.

2.8.3 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617) 256-9013. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

2.8.4 TROUBLE ANALYSIS

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle.

No Operation

Failure of the unit to operate or of the power switch indicator to light in the on (in) position may be caused by:

1. Lack of AC power to the wall receptacle (check its breaker or measure its voltage).
2. Failure of fuse replace with a known good fuse, 3A Slo-Blo for 120V, 1.5A Slo-Blo for 220 or 240V). Refer to Section 2.3, INPUT POWER CONNECTIONS, for fuse removal.
3. Range card is in the wrong position. Refer to Section 2.3, INPUT POWER CONNECTIONS, for card removal.

Erratic Operation

Erratic operation of the unit may be due to failure or partial failure of the DC power supply.

2.8.5 OUTPUT CHARACTERISTICS

Minimum DC value of Ripple at low line. (Low line = 103.5VAC in 117VAC mode.)

Supply	ØA	2A	4A	5A	8A
+34V	+30V	+27V			
+17V	+15V			+10.5V	
-34V	-30V	-28V			
-17V	-15V				-11V

2.8.6 MODULE LOADS

Current Required in A

Module	+34V	+17V	-34V	-17V
MS-302	.05	0.5	.05	1.5
MN-302	N/A	1.0	N/A	2.7
MB-302	N/A	1.1	N/A	4.3

2.8.7 TEST PROCEDURE

Equipment Required

The specifications given are those necessary to perform the tests and are not necessarily those of the suggested equipment.

a. Oscilloscope

Tektronix 7104 with 7A29 vertical plug-in and 7B10/7B15 horizontal plug-in or equivalent.

Procedure

1. Initial Setup

Remove the top cover and baffle. Insert a full complement of modules and connect the MF-5 to a variable AC line.

DANGER: Hazardous voltages exist in this equipment. Stay clear of all line-voltage wiring and terminals.

2. Pilot Lamp, Fans

Turn on power. Indicator lamp in power switch must light and both fans must turn at maximum rpm.

Replace the top cover and baffle. Ensure that the slotted end is facing the front panel, otherwise proper circulation will not be realized.

2.8.8 GPIB

Verify that the PWR LED indicator is lit. Refer to Section 6.2, MF-5 FRONT PANEL (GPIB), for location of PWR indicator. If the PWR indicator does not light, refer to Section 2.8.4, TROUBLE ANALYSIS, for troubleshooting steps, otherwise consult factory for further details.

3. MS-302 CLOCK SOURCE

3.1 DESCRIPTION

The MS-302 Clock Source is a quarter-size TMI module that generates a clock signal variable from 1kHz to 325MHz. This module is designed for use in Tau-Tron Modular Instrumentation (TMI).

Voltage-controlled oscillators and frequency dividers are used to generate the continuously variable output frequency. In addition, up to three separate crystal frequencies may be specified as an option for applications where high stability, fixed frequency signals are required.

A six-digit display inducts the output frequency, other features include dual outputs with selectable output signal levels and GPIB which is available as an option.

The MS-302 requires the Tau-Tron MF-5 Mainframe for operating voltages and cooling.

3.2 SPECIFICATIONS

Frequency Range	1kHz to 325MHz, variable using coarse range select and VCO tuning for continuous coverage.
Crystal Options	From one to three different crystals may be ordered, the frequency may be selected in the range of 1kHz to 325MHz. Options: OP-04-X: Crystal Oscillator (X = specific frequency or frequencies).
Output signal	Amplitude: Selectable, 1V into 50 ohms to ground (TMI) or ECL into 50 ohms to -2V. An internally mounted select switch is used. Rise/Fall Time: 700ps maximum, ±7% maximum distortion when driving 50-ohm DC load. Waveshape: Squarewave.
Output Channels	Two identical output amplifiers drive the BNC front-panel connectors. Each channel has independent selection of output amplitude.
Options	OP-02 IEEE-488 Interface (GPIB) OP-04-X Crystal Oscillator (X=specific frequency or frequencies).
Power	+34V -34V +17V -17V
Cooling	Forced air, supplied by mainframe.
Mechanical	TMI quarter-size module. DIMENSIONS: 6.375 in. high x 4 in. wide x 11 in. deep. WEIGHT: 2 lb net, 5 lb shipping.

3.3 INSTALLATION

Module Insertion

1. Pull out the Module Lock knob on the MF-5.
2. Insert the module as required.
3. Push in the Module Lock knob.

The module(s) can be inserted in any position desired. In general, systems shipped by Tau-Tron have modules inserted in the following order:

Position 1...Clock
Position 2...Transmitter
Position 3...Receiver

Module Removal

1. Pull out the Module Lock knob.
2. Grasp the module to be removed by its front-panel thumbscrews and pull to remove.
3. Push in the Module Lock knob to prevent the remaining modules from accidentally falling out.

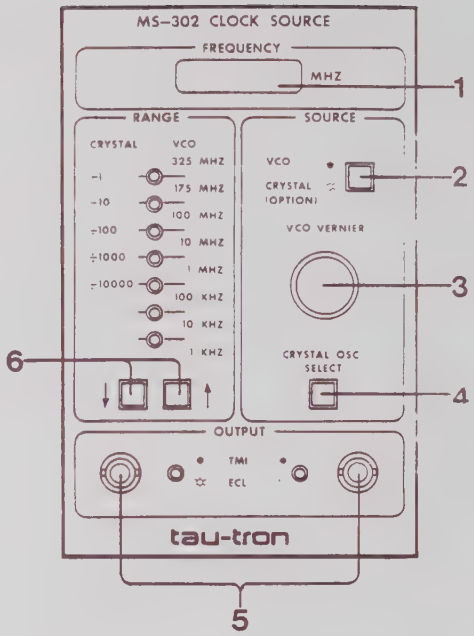
Crystal Oscillator Selection

When two or more crystal-controlled oscillators are installed, only one at a time can be placed in-circuit by the front-panel VCO crystal switch.

Interconnections

The MS-302 OUTPUT is normally connected to the input of a generator by means of a 50-ohm BNC cable of the shortest practical length.

3.4 FRONT PANEL



1 FREQUENCY — Six-digit LED display shows the frequency of the signal at the output jack. The frequency is shown as "XXX.XXXMHz".

2 VCO/CRYSTAL (Option) — Illuminated pushbutton selects the source of the output signal between the internal voltage controlled oscillator or one of three specified crystal oscillators. The pushbutton is not lit when VCO is selected but lit when crystal is selected. The crystal-controlled mode of operation is optional (OP-04-X) and can include up to three crystal-controlled oscillators. Only one of three oscillators at a time can be placed in circuit by the VCO CRYSTAL switch.

3 VCO VERNIER — Control knob sets the output frequency in the VCO mode. The range of this control is from less than 100MHz to greater than 325MHz in two steps. In all other selections the control covers a 10 to 1 frequency range.

4 CRYSTAL OSC. SELECT — Pushbutton indicator selects one of three internal crystal oscillators when the Crystal Source is selected. Push the button until the proper frequency is shown on the FREQUENCY DISPLAY to get the desired crystal.

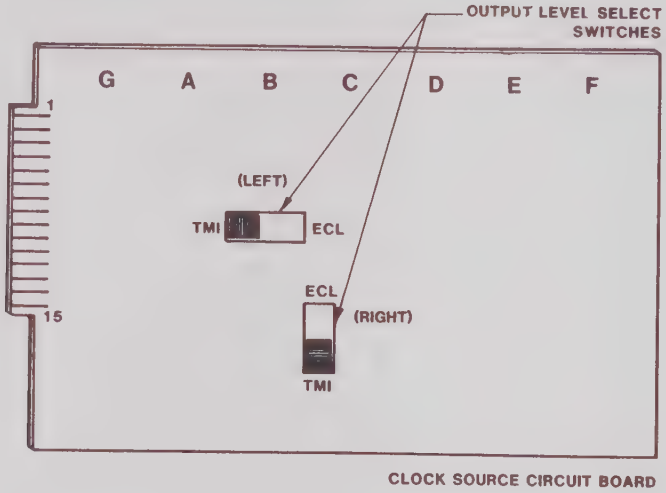
5 OUTPUT — Two BNC connectors provide simultaneous output signals. Internally mounted printed-circuit board switches allow the selection of two output levels. In the TMI mode (indicators not lit) the signal amplitude is 1V into 50 ohms to ground terminating resistor.

		In the ECL mode (indicators lit) the signal swing is compatible with ECL circuit inputs. The termination must be 50 ohms to -2V. In either case the rise and fall times are typically 500 pico-seconds.
6	Range Increment/ Decrement Select	Two illuminated pushbuttons set the VCO tuning range at the output. The selected range is indicated by an illuminated LED. When in the CRYSTAL mode, one of five dividers may be selected (÷1,÷10,÷100, ÷1000, and ÷10000). In all cases the frequency at the module output is displayed.

3.5 OPERATION

3.5.1 OUTPUT LEVEL SELECT

Remove the module from the mainframe, the OUTPUT LEVEL SELECT switches are located on the Clock Source circuit board. Each channel may be independently selected by means of the two printed circuit mounted slide switches. Make the proper level selection, return the module to the mainframe.



3.5.2 CONTINUOUS FREQUENCY SELECT

Any output frequency between 1kHz and 325MHz can be selected as follows:

1. Set the VCO/CRYSTAL pushbutton to VCO.
2. Set the RANGE with the range select pushbuttons as determined by the associated VCO RANGE display.
3. Set the VCO VERNIER control to the desired frequency as shown on the FREQUENCY display.

3.5.3 CRYSTAL FREQUENCY SELECT

1. Set the VCO/CRYSTAL pushbutton to CRYSTAL the pushbutton should latch and the LED should be ON.
2. Set the RANGE control pushbuttons to the desired crystal divisor as determined by the CRYSTAL DIVISOR table, ÷1; ÷10; ÷100; ÷1000; ÷10000.
3. Select the desired crystal frequency (in case of more than one crystal oscillator) using the CRYSTAL OSC. SELECT pushbutton. Check the selected oscillator by observing the FREQUENCY display.

NOTE: The FREQUENCY display always reads the final output frequency, if a crystal divisor other than ÷1 is selected, the display will show the divided frequency.

3.6 THEORY OF OPERATION

3.6.1 CLOCK SOURCE BOARD

The MS-302 uses two voltage controlled oscillators (VCOs) and a series of decade dividers to generate the output frequency. One of the oscillators covers a 2:1 frequency range of about 175 to 350MHz, this provides the highest frequency range of 325MHz. A divide-by-two circuit at the VCO output generates the next lowest range of 100 to 175MHz. Because of the divide-by-two at this point, the actual frequency range is actually about 85 to 175MHz.

The second VCO tunes a 10:1 range from 10 to 100MHZ, decade frequency dividers are then used to select the remaining frequency bands.

The RANGE Select pushbuttons control an up-down binary counter whose outputs drive the select lines of an 8 to 1 multiplexer/selector.

It should be noted that, in order to minimize signal interference from unused oscillators, the unused oscillators are shut off by removing the DC voltage from the oscillator input.

The Crystal Oscillators are selected by a similar counting circuit and a 3 to 1 multiplexer/selector which enables only one crystal oscillator at a time. All other crystal oscillators and the two voltage controlled oscillators are shut off when they are not selected.

The output signals are developed by high-speed micro-circuit switching amplifiers. The output levels are selected by slide switches mounted on the Clock Source printed-circuit board. These amplifiers are DC coupled at the output and must drive DC coupled 50-ohm loads. The load can either be 50 ohms to ground in the case of TMI or 50 ohms to -2 volts in the case of ECL. The important point is that the load must be direct coupled in order to minimize waveshape distortion.

3.6.2 FRONT-PANEL DISPLAY BOARD

A universal frequency counter, LED driven integrated circuit drives the FREQUENCY display. The input to the counter comes from a divide-by-100 circuit at the output of the RANGE SELECTOR so that the displayed value always represents the frequency of the final output signal.

3.6.3 MODULE POWER SUPPLIES

The unregulated mainframe voltages of ±34V and ±17V are the inputs to voltage regulators located on the rear and side of the module. The +34V and -34V drive +15 and -15V regulators with loads of much less than 1A . The +17V is regulated to +8V which provides power to the micro-circuit amplifiers and is also the input to a +5V regulator located on the Clock Source board. This voltage is used for TTL logic circuit power. The -17V is regulated to a -5.2V high current supply using a combination of a three-terminal regulator and boost transistor. This voltage is also used to drive a PC board mounted -2V regulator which supplies the termination voltage for the high-speed ECL circuits.

3.7 GPIB OPTION

General

All front-panel controls, except the VCO VERNIER, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An associated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired

Message Format

The message consists of four digits (in ASCII code) followed by a terminator.

Ident	VCO/ CRYSTAL	CRYSTAL/ VCO RANGE	CRYSTAL OSC SELECT	Termi-nator

Ident

Digit	Meaning
1	MS-302 Clock Source

VCO/CRYSTAL

Digit	Meaning
0	CRYSTAL
1	VCO

CRYSTAL/ VCO RANGE

Digit	Meaning
0	175 to 325MHz; or full crystal frequency
1	100 to 175MHz; or crystal ÷10
2	10 to 100MHz; or crystal ÷100
3	1 to 10MHz; or crystal ÷1000
4	0.1 to 1MHz; or crystal ÷10000
5	10 to 100kHz; no output in crystal mode
6	1 to 10kHz; no output in crystal mode
7	Illegal (no output)

CRYSTAL/ OSC SELECT

Digit	Meaning
0	1st crystal frequency
1	2nd crystal frequency
2	3rd crystal frequency
3	Illegal (no output)

Terminator

Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

3.8 SERVICE

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

3.8.1 ROUTINE SERVICE

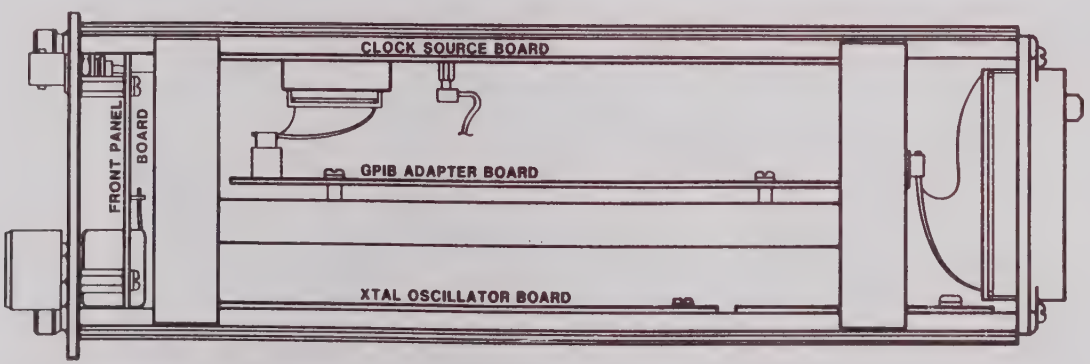
Routine service includes the performance of checks and service procedures which prevent or minimize the downtime of the unit. The checks and service are simplified, and may be limited to visual inspection for defective components, loose hardware and/or accumulation of dust within the unit at critical areas.

NOTE: It is recommended that periodic cleaning (approximately once every three months) of the interior and exterior of the unit be done with a vacuum cleaner.

Refer to Section 3.3, INSTALLATION, for module removal.

Board Seating

Ensure that all printed cicuit boards are securely seated in their connectors as shown in the illustration below.



MS-302

3.8.2 REPAIR RETURNS

For mechanical damage or electrical malfunctions, refer to Page ii, REPAIR RETURNS.

3.8.3 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617) 256-9013. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

3.8.4 TROUBLE ANALYSIS

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

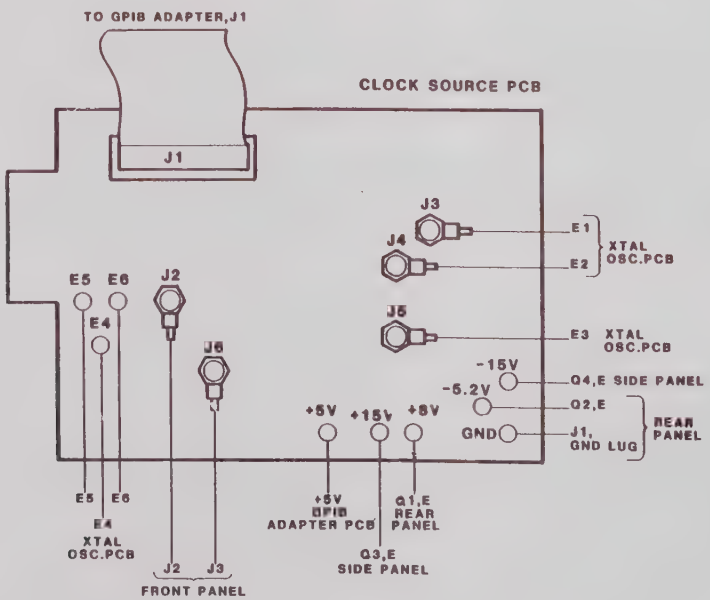
Output Levels

Verify that selected output levels are correct by observing the front panel; TMI output (LED not lit), ECL output (LED lit). Refer to Section 3.5.1 OUTPUT LEVEL SELECT, for proper TMI/ECL settings.

DC Voltages

WARNING: While measuring the -5.2V DC power supply, ensure that utmost care is taken. A power supply could be either severely damaged or completely destroyed if it is accidentally shorted to ground.

Verify that the DC votages are correct by measuring them on the Clock Source circuit board. Refer to the illustration below for the proper measurement points.



If the correct voltages are not indicated, consult the factory.

Calibration

Routine calibration is not normally required except in the following situations:

a. Failed component or circuit. Consult factory for further details.
b. Failure of LED indicator(s) to light if determined to be functional; measure the outputs with an oscilloscope (Tektronix 7104 or equivalent) and verify their signal outputs according to Section 3.2, SPECIFICATIONS. (Consult factory if signal outputs are not correct.)
c. Harsh environment; typical environment is:

Temperature	32 to 95°F (0 to 35°C)
Humidity	0 to 95% RH max at 20°C, non-condensing.

Any calibrations or technical adjustments other than the situations mentioned above should not be made during the Warranty period unless otherwise authorized. Consult factory for further details. (Refer to sections 3.2 and 3.5, SPECIFICATIONS and OPERATION, respectively, for proper switch, control, level and LED indicator settings.)

4. MN-302 BERT TRANSMITTER

4.1 DESCRIPTION

The Tau-Tron MN-302 BERT Transmitter is a quarter-size TMI module that generates either pseudorandom data patterns or 16-bit word patterns. Four different pseudo-random data patterns are available as well as four 16-bit patterns. The MN-302 must be driven from an external clock source such as the MS-302, and operates over the range of 1kHz to 325MHz.

Selectable input and output termination voltages and amplitudes make the MN-302 compatible with a variety of standard high-speed circuits and systems. Other features such as a delayed data output, clock output, error inject and frame sync signals provide increased versatility and ease of operation.

The MN-302 requires the Tau-Tron MF-5 Mainframe for operating voltages and cooling.

4.2 SPECIFICATIONS

Clock Input — 1kHz to 325MHz range with the following signal type selections:

TMI-- 1V amplitude, input impedance is direct coupled 50 ohms to ground. For use with other TMI modules or signal source generating this type of signal.

ECL-- 0.8V amplitude, input impedance is direct coupled 50 ohms to -2.0V.

AC--- 1V amplitude, AC coupled 50-ohm load, 1MHz low frequency limit.

The clock waveshape should be approximately 50% duty cycle.

Data Inhibit — TTL input of 2V min into 1k ohms to +5V at front-panel BNC connector, low-level active, 50ns min pulse width. Synchronously gates off output data, forcing output to logic-0; does not affect code generator.

Data Pattern — Pseudorandom with choice of 4 front-panel selected lengths of 2^7-1(127), 2^{15}-1(32,767), 2^{20}-1(1,048,576), or 2^{23}-1(8,388,607) bits per frame or four fixed 16-bit words, A: Alternating 1-0; B, C, and D: random.

Error Injection — Internal or External, LED indicated. Internal: OFF or 2 errors per 100 data bits. External: TTL input of 2V into 1k ohms to +5V, front-panel BNC connector; logic-0 to logic-1 level triggers one-bit error; min pulse width of 50ns or 2 clock periods, whichever is longer.

Data Output — NRZ/RZ format. Internally selected as TMI signal of 1V into 50 ohms to ground or as ECL signal of 1V into 50 ohms to -2V; available at front-panel BNC connector.

Delayed Data Output — NRZ format, delayed 8 bits from Data Output. Front-panel controlled as true or complement signal, internally selected TMI output of 1V into 50 ohms or as ECL output of 1V into 50 ohms to -2V; available at front-panel BNC connector.

Clock Output — Waveshape follows clock input. Internally selected as TMI signal of 1V into 50 ohms to ground or as ECL singal of 1V into 50 ohms to -2V.

Sync Output	Squarewave output occurs once every 4 pseudorandom sequences for 2^7-1, 2^{15}-1, and 2^{23}-1. Pulse occurring once every 2 pseudorandom sequences for 2^{20}-1. Squarewave occurring once every 4 fixed words for words A and B, once every 8 fixed words for words C and D.
Options	OP-02 IEEE-488 Interface (GPIB)
Power	+17V nominal at 0.3A, -17V nominal at 1.2A, unregulated and supplied by mainframe.
Cooling	Forced air, supplied by mainframe.
Mechanical	TMI quarter-size module. DIMENSIONS: 6.375 in. high x 4 in. wide x 11 in. deep. WEIGHT: 2 lb net, 5 lb shipping.

4.3 INSTALLATION

Module Insertion

1. Pull out the Mainframe Module Lock knob.
2. Insert the module as required.
3. Push in the Module Lock knob.

The module(s) can be inserted in any position desired. In general, systems shipped by Tau-Tron have modules inserted in the following order:

Position 1..Clock
Position 2..Transmitter
Position 3..Receiver

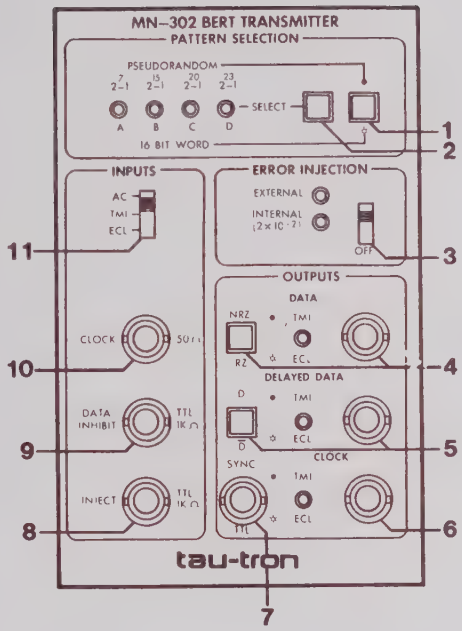
Module Removal

1. Pull out the Mainframe Module Lock knob.
2. Grasp the module to be removed by its front-panel thumbscrews and pull to remove.
3. Push in the Module Lock knob to prevent the remaining modules from accidentally falling out.

Interconnections

The CLOCK IN of the MN-302 normally connects to the output of a clock by means of a BNC terminated cable of the shortest practical length. The CLOCK OUT and DATA OUT of the MN-302 normally connect to the system under test.

4.4 FRONT PANEL



1 PSEUDORANDM/ 16-BIT WORD — Two-position illuminated pushbutton selects either pseudorandom (not lit) or 16-bit word (lit) patterns for system stimulation.

2 PATTERN SELECT — Illuminated pushbutton with LED indicators selects four pseudorandom sequence lengths 2^7-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 and fixed words: 16-bit, A: Alternating 1-0; B, C, and D: Random.

3 ERROR INJECTION — Veritcal three-position slide switch; DOWN is the OFF position, no errors injected, the CENTER position selects the internal 10^{-2} error-rate, the UP position selects an external signal to generate the errors. The INTERNAL LED will be illuminated when that mode is selected, the EXTERNAL LED illuminates each time an error signal appears at the Error Input Connector.

4 DATA Output — BNC connector with LED indicator (used in conjunction with the illuminated select switch for NRZ/RZ format indication) internally selects either a TMI (not lit) signal of 1V into 50 ohms to ground or an ECL (lit) signal of 0.8V into 50 ohms to -2V.

5 DELAYED DATA Output — BNC connector for NRZ format data with LED indicator receives a delayed 8 bits (true or complement) from the DATA Output and internally selects either a TMI (not lit) signal of 1V into 50 ohms to ground or an ECL (lit) signal of 0.8V into 50 ohms to -2V.

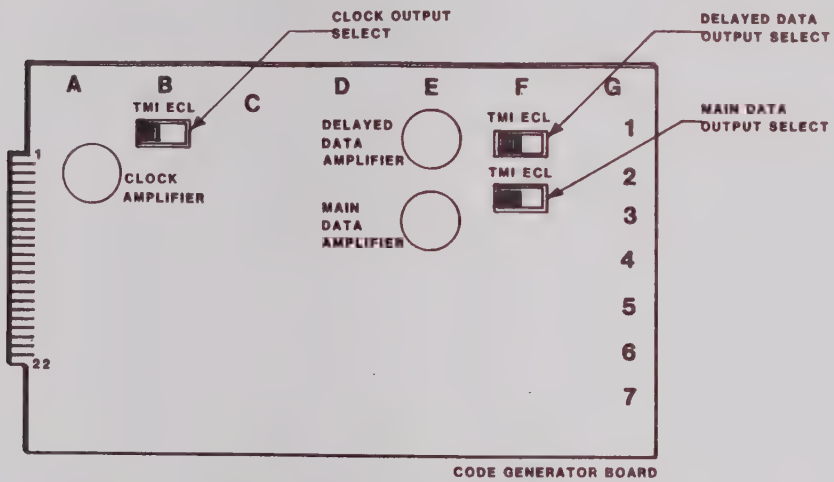
6 CLOCK Output — BNC connector with LED indicator internally selects either a TMI signal of 1V into 50 ohms to ground or an ECL signal of 0.8V into 50 ohms to -2V.

7	SYNC Output	BNC connector for sync output, as defined in section 4.2.
8	INJECT Input	BNC connector accepts external error injection input of 2V into 1k ohms to +5V with a minimum pulse width of 50ns or 2 clock periods whichever is longer.
9	DATA INHIBIT	BNC connector for TTL input at a minimum of 2V into 1k ohms at +5V with a low-level active, 50ns minimum pulse width. It synchronously gates off output data, forcing output to logic-0 while not affecting the code generator output.
10	CLOCK	BNC connector accepts either AC, TMI or ECL inputs.
11	Clock INPUTS	Veritical three-position slide switch controls AC, TMI and ECL into BNC connector. The AC, TMI inputs range from 1MHz or 1kHz, respectively, to 325MHz with 1V into 50 ohms to ground, AC and DC coupled respectively. The ECL input ranges from 1kHz to 325MHz with 0.8V into 50 ohms to -2V, DC coupled.

4.5 OPERATION

4.5.1 OUTPUT LEVEL SELECT

1. Before turning on power, pull out the PULL TO UNLOCK lever at the upper right-hand corner of the mainframe, slide the MN-302 out and set the interior slide switches for desired output levels (TMI or ECL) of DATA, DELAYED DATA and CLOCK outputs.



2. Slide the MN-302 back in and push in the PULL TO UNLOCK lever.

3. Turn on the mainframe power.

4.5.2 CLOCK INPUT CONNECTION

Use a 50-ohm BNC cable to connect the MS-302 CLOCK OUT to the MN-302 CLOCK IN.

NOTE: Be sure that the OUTPUT LEVEL selected on the MS-302 agrees with the CLOCK INPUT selected on the MN-302.

4.5.3 PATTERN SELECTION

The PSEUDORANDOM/16-BIT WORD pushbutton is used to select the output data. In the PSEUDORANDOM mode, the button is out and the indicator in the pushbutton is not lit. To select 16-BIT WORD, push the select button in, it should latch and the button should light. To restore PSEUDORANDOM, push the button and the latch should release.

4.5.3.1 PATTERN SELECT INDICATORS

These indicators perform two functions; one is to indicate which pattern has been chosen, the other indicates the presence of an acceptable input clock. If no pattern select light is on after the clock signal has been connected, then the clock signal amplitude, period, and symmetry should be checked with an oscilloscope whose bandwidth is compatible with the signal being observed.

NOTE: To ensure that the proper pseudorandom sequence is being generated, check the sync period. The exact sync period for each pseudorandom sequence is as follows:

Pseudorandom Sequence at 100MHz

2^7-1, 5.1us squarewave
2^{15}-1, 1.3ms squarewave
2^{20}-1, 21ms pulse
2^{23}-1, 335ms squarewave

Fixed Word at 100MHz

A...640ns squarewave
B...640ns squarewave
C...1280ns squarewave
D...1280ns squarewave

4.5.4 ERROR INJECT

To select the internal error inject rate of 2×10^{-2}, put the ERROR INJECTION switch to the CENTER position. The INTERNAL LED should be illuminated. To select EXTERNAL INJECTION, put the slide switch in the upper-most position and connect the error inject signal to the INJECT BNC connector. The EXTERNAL LED will light each time the INJECT signal goes from logic-0 to logic-1.

4.5.5 SYSTEM UNDER TEST CONNECTION

After all of the desired signal conditions have been set, make the required connections to the system under test. All connections must be made with 50-ohm coaxial cable with BNC connectors.

4.5.6 OSCILLOSCOPE USE

The FRAME SYNC output on the MN-302 provides an output which can be used to synchronize an oscilloscope in order to observe the output data pattern. The data pattern must be connected to the oscilloscope with a 50-ohm coaxial cable and the oscilloscope veritcal input must be terminated with 50 ohms. It should be noted that the longer code lengths such as 2^{15}-1, 2^{20}-1 and 2^{23}-1 have extremely long frame sync periods and are difficult to observe on an oscilloscope. The easiest pattern to observe is the 2^{7}-1 or short sequence.

4.6 THEORY OF OPERATION (Refer to System Block Diagram)

The MN-302 consists of four main signal processing sections; the input clock amplifier and clock distribution, the pattern generator, the control functions and the output amplifiers. An additional function of the module is to convert the unregulated mainframe voltage into regulated voltage for use within the module.

4.6.1 INPUT CLOCK AMPLIFIER AND CLOCK DISTRIBUTION

A wide-band input amplifier converts either of the three selectable input levels to ECL for use within the system. An internal threshold adjustment is factory-set for maximum sensitivity and frequency response. The input clock drives a high-speed divide-by-two for distribution to the logic circuits which run at a half rate. The input clock also drives the output data latch for final signal shaping at full rate and the RZ select gate which, when enabled, generates the RZ output on the MAIN DATA port.

4.6.2 PATTERN GENERATOR

The MN-302 pattern generator is a variable length linear feedback shift register with taps chosen such that the output data stream is a maximal-length pseudorandom sequence. In order to minimize the distribution of the high-speed clock signals, all code generating logic is run at half rate, then combined and doubled to produce the final output data at full rate. The only high-speed clock (full rate) is at the output data latch where all switching distortion from the rate multiplier (Multiplexer) is removed.

4.6.2.1 FRAME SYNC COUNTER AND ALL ZEROS DETECTOR

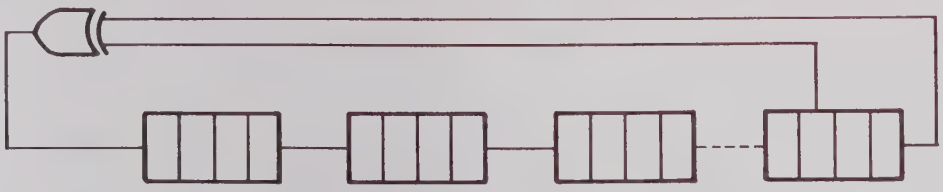
In order to generate a sync pulse on a per frame basis, the Frame Sync Counter detects a unique bit pattern within the frame period of the selected code. This unique pattern is the maximum number of consecutive zeros which, in this type of pattern generator is always one less than the number of stages in the shift register. In the case of the 2^7-1 code length, there are seven stages in the shift register, hence six consecutive zeros occur, but occur only once in the 127-bit frame length. The same analysis holds true for the remaining code lengths except that the number of bits per frame, and hence the time between frames, is considerably longer.

The ALL ZEROS DETECTOR is a natural extension of the Frame Sync Counter. If the shift register reaches the all zeros state, then further shifting will be inhibited. In order to guard against this condition, which may occur as a result of power turn-on transients or pattern selection transients, the ALL ZEROS Detector will generate a pulse to the shift register, forcing it to the ALL ONES state where normal shifting can resume.

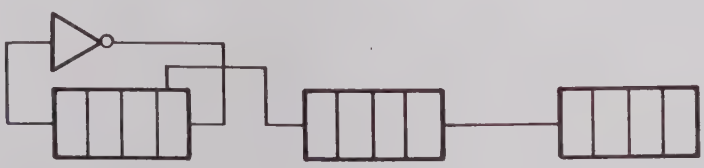
4.6.2.2 FIXED WORD PATTERN

The MN-302 can produce four fixed patterns of 16-bit words under control of the 16-bit word selection on the front panel. When this latching pushbutton is pushed, its LED indicator will light; the pattern selector can now be set to A, B, C or D. If Fixed Word A is selected then the MN-302 output will be an alternating one/zero pattern. If any of the other fixed words are selected, the output will be an undefined 16-bit word; also, if a change of 16-bit word is made such as selecting B, then C and back to B, the second selection if B, may not be the same as the first selection.

This is because of the mechanism of generating the fixed word patterns:



In the pseudorandom mode, the shift register, consisting of blocks of 4-bit universal shift registers looks like the above diagram. When a 16-bit word is selected, the diagram changes as follows:



Notice that the first 4-bit block becomes a 4-bit shift register with inverted feedback. This means that whatever state the 4-bits were in when the Fixed Word was selected remains in the circulating 4-bit register. If the pattern is changed via the front-panel control, then these 4 bits will be in some other state when the word is selected. Thus, some other pattern will appear at the output.

The 16-bit word under selection A is the only predictable output. In this mode, the state of the inverted 4-bit shift register is ignored and the half-rate clock is fed directly to the output latch where it is strobed by the full-rate clock, resulting in an alternating one/zero pattern at the output.

4.6.3 CONTROL FUNCTIONS

A series of signals controlled by the front panel enable various internal functions on the Code Generator card. They include the Error Inject functions, NRZ/RZ select, DATA or $\overline{\text{DATA}}$, and the Data Inhibit function.

4.6.3.1 ERROR INJECT

There are two methods for injecting errors into the output data stream, they are INTERNAL and EXTERNAL. In either case, the error signal is synchronized with one channel of the pattern generator running at half the clock rate. The synchronization logic generates a pulse exactly one bit wide at the half rate each time a logic-0 to logic-1 transition occurs at the synchronization logic input. This pulse and one channel of the half-rate data are inputs to an Exclusive-OR gate; each time an error pulse is received at this gate, a bit in the data stream is inverted, resulting in an error at the output.

INTERNAL Error inject is generated by a divide-by-25 on the half-rate clock. This generates one error pulse every 50 bits in the data stream or two errors every 100 bits resulting in the 2×10^{-2} internal error-rate.

EXTERNAL Error Inject synchronizes logic-0 to logic-1 data transitions at the front-panel INJECT input with the pattern generator by using the half-rate clock and high-speed flip-flops. Each time the external error signal makes a low to high transition, an error pulse will be generated at the Exclusive-OR gate input which will invert one bit in the data stream. The width of the external error signal must be at least twice the width of the input clock period.

4.6.3.2 NRZ/RZ

The MAIN DATA output has two data formats available as selected by the front-panel NRZ/RZ pushbutton. In the NRZ mode, a logic-1 occupies the entire clock period; in the RZ mode the data are logically combined with the full-rate system clock such that a logic-1 in the output data is approximately equivalent to the width of the logic-1 component of the clock.

4.6.3.3 DATA/$\overline{\text{DATA}}$

The DELAYED DATA output can be either normal (true) or inverted as a function of this switch. This is accomplished by simply inverting the delayed data stream by means of a DC voltage at the input to an Exclusive-OR gate. DATA places a logic one voltage at this gate which inverts the entire data stream.

4.6.3.4 DATA INHIBIT

This function, which is active LOW, forces both the Main Data and the Delayed Data outputs to logic-0 for the duration of the low (TTL ZERO) at the front-panel input. The signal is clocked by a flip-flop whose output either enables or inhibits the data pattern. The actual pattern generator is not affected by the Data Inhibit function, only the output is driven to logic-0.

4.6.4 OUTPUT AMPLIFIERS

Three identical high-speed switching amplifiers generate the DATA, DELAYED DATA and CLOCK output signals. These amplifiers are capable of high switching speed, fast transition time, and minimum waveshape distortion when driving 50-ohm loads. The TMI/ECL level setting, which is selected by a front-panel switch, changes bias voltages on the output amplifiers such that the termination potential can either be ground or -2V.

4.6.5 MODULE POWER SUPPLIES

The MN-302 uses the +17V and -17V unregulated mainframe voltages to generate +8V and -5.2V on the module rear panel. The Code Generator board develops +5V from the +8 and generates -2V from the -5.2 by using three-terminal regulators mounted on the board. Because of the current required from the -5.2V, a boost transistor is mounted on the side panel, providing increased current capacitiy to the -5.2V regulator.

4.7 GPIB OPTION

General

All front-panel controls, except the Clock INPUT slide switch, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An asscociated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired.

Message Format

The message consists of five digits (in ASCII code) followed by a terminator.

Ident	ERR INJ	PATTERN	RZ/NRZ DATA	D/$\overline{D}$ DLY DATA	Termi-nator

Ident

Digit	Meaning
2	MN-302

ERR INJ

Digit	Meaning
0	OFF
1	Internal Error Injection
2	External Error Injection
3	Illegal

PATTERN

Digit	Meaning
0	2^7-1 pseudorandom pattern
1	2^{15}-1 pseudorandom pattern
2	2^{20}-1 pseudorandom pattern
3	2^{23}-1 pseudorandom pattern
4	16-bit pattern A
5	16-bit pattern B
6	16-bit pattern C
7	16-bit pattern D

RZ/NRZ DATA

Digit	Meaning
0	RZ DATA
1	NRZ DATA

D/$\overline{D}$ DELAYED DATA

Digit	Meaning
0	$\overline{D}$ DELAYED DATA
1	D DELAYED DATA

TERMINATOR

Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

4.8 SERVICE

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

4.8.1 ROUTINE SERVICE

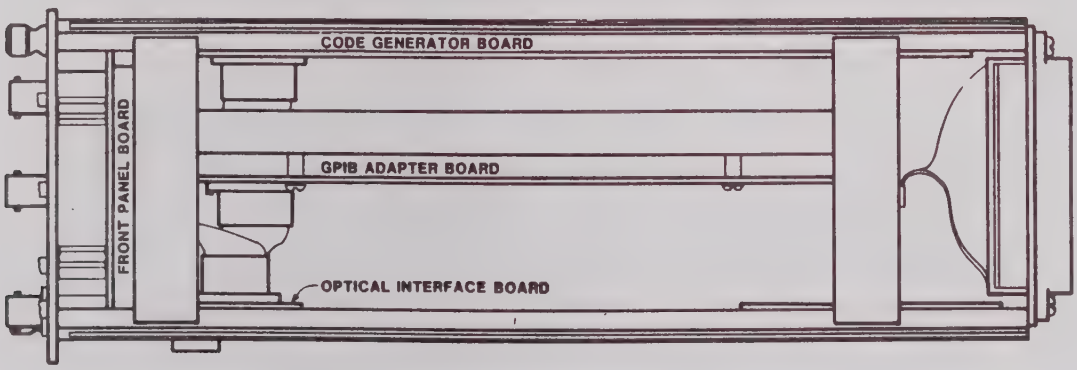
Routine service includes the performance of checks and service procedures which prevent or minimize the downtime of the unit. The checks and service are simplified, and may be limited to visual inspection for defective components, loose hardware and/or accumulation of dust within the unit at critical areas.

NOTE: It is recommended that periodic cleaning (approximately once every three months) of the interior and exterior of the unit be done with a vacuum cleaner.

Refer to Section 4.3, INSTALLATION, for module removal.

Board Seating

Ensure that all printed cicuit boards are securely seated in their connectors as shown in the illustration below.



4.8.2 REPAIR RETURNS

For mechanical damage or electrical malfunctions, refer to Page ii, REPAIR RETURNS.

4.8.3 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617) 256-9013. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

4.8.4 TROUBLE ANALYSIS

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

Output Levels

Verify that selected levels are correct by observing the front panel; TMI DATA, DELAYED DATA and CLOCK outputs (LEDs not lit), ECL DATA, DELAYED DATA and CLOCK outputs (LEDs lit). Refer to Section 4.5.1, OUTPUT LEVEL SELECT, for proper TMI/ECL settings.

Clock Input Connection

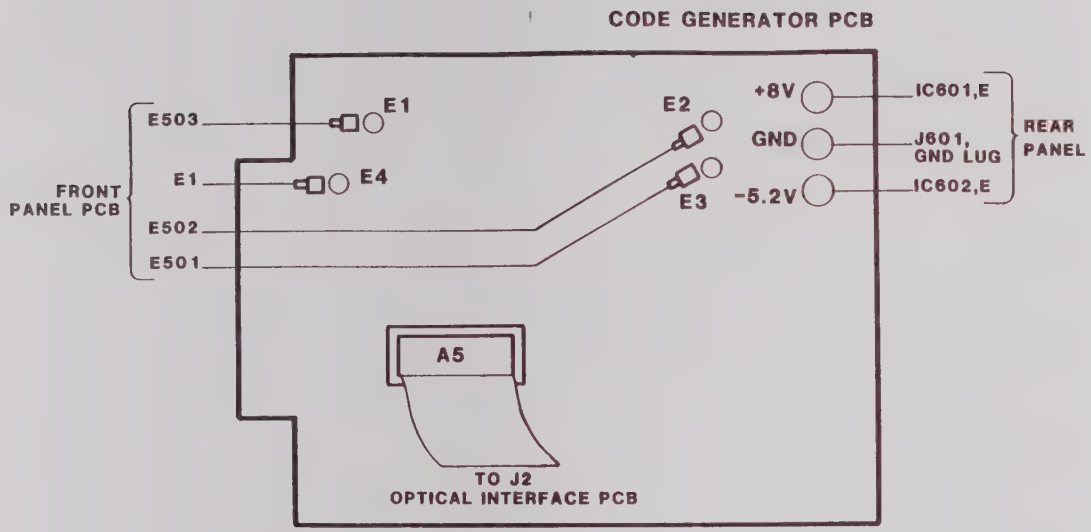
Verify that selected OUTPUT LEVEL on the MS-302 agrees with the CLOCK INPUT selected; i.e., TMI for TMI and ECL for ECL.

To verify all other settings, refer to Pages 4-8 and 4-9.

DC Voltages

WARNING: While measuring the -5.2V DC power supply, ensure that utmost care is taken. A power supply could be either severely damaged or completely destroyed if it is accidentally shorted to ground.

Verify that the DC votages are correct by measuring them on the Code Generator circuit board. Refer to the illustration on the following page for the proper measurement points.



If the correct voltages are not indicated, consult the factory.

Calibration

Routine calibration is not normally required except in the following situations:

a. Failed component or circuit. Consult factory for further details.

b. Failure of LED indicator(s) to light if determined to be functional; measure the outputs with an oscilloscope (Tektronix 7104 or equivalent) and verify their signal outputs according to Section 4.2, SPECIFICATIONS. (Consult factory if signal outputs are not correct.)

c. Harsh environment; typical environment is:

Temperature	32 to 95°F (0 to 35°C)
Humidity	0 to 95% RH max at 20°C, non-condensing.

Any calibrations or technical adjustments other than the situations mentioned above should not be made during the Warranty period unless otherwise authorized. Consult factory for further details. (Refer to sections 4.2 and 4.5, SPECIFICATIONS and OPERATION, respectively, for proper switch, control, level and LED indicator settings.)

5. MB-302 BERT RECEIVER

5.1 DESCRIPTION

The Tau-Tron MB-302 BERT RECEIVER is a half-size TMI module that provides error-detection and error-measurement capabilities. It not only generates internal pseudorandom and fixed-word references but also allows the application of an externally applied reference for special requirements.

Four modes of operation are provided, including one that automatically selects the type of reference pattern being received and automatically synchronizes on it. Four different measurements are provided, each with switch selectable display times of 1 second, 10 seconds or hold. In one measurement, detected errors are counted and displayed as total errors up to six digits, plus overflow. Two measurements display the error-rate, one with and one without automatic range selection of 10^{-2} through 10^{-9}. The fourth measurement is that of the input clock frequency, in MHz with 1kHz resolution. All measurements are indicated on a large, bright, and easily-read display. The data are also available at a rear-panel connector for automatic logging.

The MB-302 requires the Tau-Tron MF-5 Mainframe for operating voltages and cooling.

5.2 SPECIFICATIONS

CLOCK Input	1kHz to 325MHz range with the following signal type selections: TMI-- 1V amplitude, input impedance is direct coupled 50 ohms to ground. For use with other TMI modules or signal source generating this type of signal. ECL-- 0.8V amplitude, input impedance is direct coupled 50 ohms to -2.0V. AC--- 1V amplitude, AC coupled 50-ohm load, 1MHz low frequency limit. The clock waveshape should be approximately 50% duty cycle.
DATA Input	Choice of TMI, ECL or AC coupling (see CLOCK Input), front-panel controlled, into front-panel BNC connector. Front-panel PHASE control selects additional 3 steps of delay of input data relative to clock for proper clock/data phasing, approximately 3ns max delay.
REFERENCE DATA Input	1kHz to 325MHz, ECL level of 0.8V into 50 ohms to -2V. Must be externally aligned, bit-by-bit, with data input.
COMMAND Input	TTL level of 2V min into 1k ohms to +5V; with burst-mode off, rising edge of this input triggers receiver synchronization. With burst-mode on, low level of this input inhibits error measurement and synchronization checking; and rising edge triggers synchronization (if necessary).
DATA Patterns	Pseudorandom, fixed word or external data. Pseudorandom at 2^7-1 (127), 2^{15}-1 (32,767), 2^{20}-1 (1,098,575), or 2^{23}-1 (8,388,607) bits. Fixed word of any 16-bit repetitive pattern. External data of external synchronized reference pattern.
Synchronization	Four modes are available; automatic, manual, external and external reference data, as selected by front-panel pushbuttons and indicated by front-panel LEDs.
Measurements	Four modes are available, as selected by front-panel pushbuttons and indicated by front-panel LEDs. Display times of 1s, 10s, or hold may be selected. An LED indicates when a measurement is in progress. The RESET pushbutton resets the counter, display and SYNC LOST LED.

Display	6-digit, high-brightness LED display, with 0.430 in. high digits and 0.280 in. high exponent provides measurement data.
Error Output	One pulse per bit error, width follows clock input width, at ECL level of 0.8V into 50 ohms to -2V, available at front-panel BNC connector.
Sync Output	Squarewave occurring once every 4 pseudorandom sequences or every 4 16-bit fixed words, TTL level of 2.4V min into standard TTL load.
Printer Output	TTL compatible I/O lines, positive true outputs and negative true input, available at rear-panel 50-pin D-connector for use with external printer.
Options	OP-02 IEEE-488 Interface (GPIB)
Power	+17V nominal at 0.2A, -17V nominal at 6.0A, unregulated and supplied by mainframe.
Cooling	Forced air, supplied by mainframe.
Mechanical	TMI half-size module. DIMENSIONS: 6.375 in. high x 8 in. wide x 11 in. deep. WEIGHT: 12 lb net, 14 lb shipping.

5.3 INSTALLATION

Module Insertion

1. Pull out the Mainframe Module Lock knob.
2. Insert the module as required.
3. Push in the Mainframe Module Lock knob.

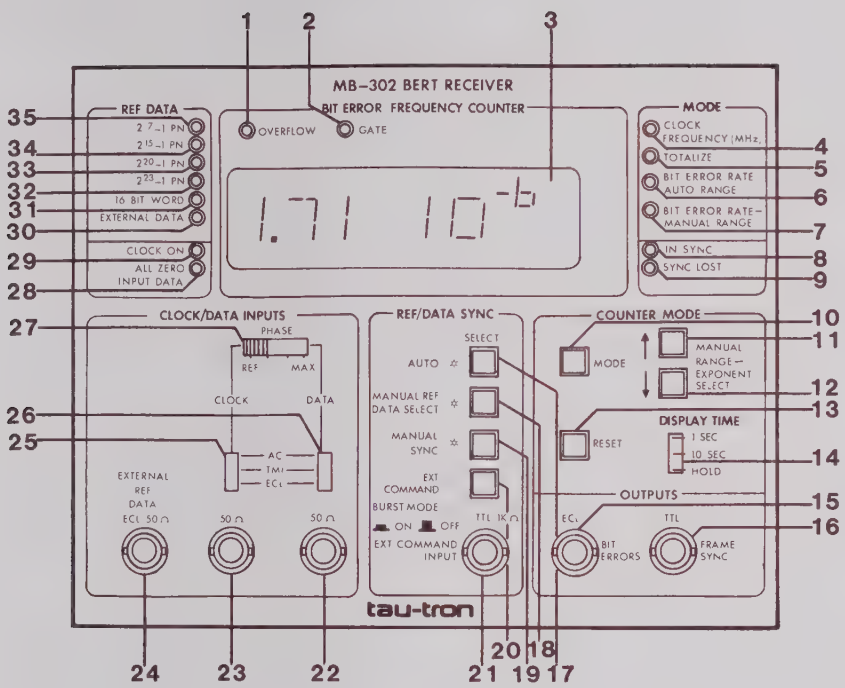
The module(s) can be inserted in any position desired. In general, systems shipped by Tau-Tron have modules inserted in the following order:

Position 1...Clock
Position 2...Transmitter
Position 3...Receiver

Module Removal

1. Pull out the Module Lock knob.
2. Grasp the module to be removed by its front-panel thumbscrews and pull to remove.
3. Push in the Module Lock knob to prevent the remaining modules from accidentally falling out.

5.4 FRONT PANEL



1 OVERFLOW — LED lights when BIT ERROR/FREQUENCY COUNTER overflows.

History vs Current Status — The original design of the MB-302 implemented the overflow indication as a "History Status"; i.e., once the display overflows, it is necessary to push the RESET button on the front panel to extinguish the OVERFLOW LED. The newer MB-302 provides for both History and Current Status OVERFLOW LEDs. In the Current Status overflow indication, the OVERFLOW LED lights if the current displayed measurement had not overflowed.

In the newer MB-302, the Counter PCB includes a shorting connector and programming pins along the edge of the board next to the front panel. As shipped from the factory the shorting connector is installed for a History indication but can be moved in the field for Current indication.

MB-302s shipped prior to October 1981, can be modified for a Current Status overflow indication. Consult factory for further details.

2 GATE — LED lights while the measurement of CLOCK FREQUENCY, TOTAL ERRORS, ERROR RATE AUTO, and ERROR RATE MANUAL are in progress.

3	Display	Indicates the number of total errors accumulated, up to 6 digits plus overflow, and the frequency in MHz, up to 6 digits plus overflow with 1kHz resolution.
4	CLOCK FREQUENCY (MHz)	LED lights when the MODE button is pushed. This button must be continuously pushed until the CLOCK FREQUENCY LED lights. The display indicates the frequency.
5	TOTALIZE	LED lights when the MODE button is pushed. This button must be continuously pushed until the TOTALIZE LED lights. The display indicates the number of total errors accumulated after the RESET button is pushed.
6	BIT ERROR RATE AUTO RANGE	LED lights when the MODE button is pushed. This button must be continuously pushed until the BIT ERROR RATE AUTO RANGE LED lights. In this mode, the display indicates the error-rate up to 3 digits plus overflow with a 2-digit exponent.
7	BIT ERROR RATE MANUAL RANGE	LED lights when the MODE button is pushed. This button must be continuously pushed until the BIT ERROR RATE MANUAL RANGE LED lights and the two MANUAL RANGE EXPONENT SELECT buttons light. The display indicates the error-rate up to 3 digits plus overflow with a 2-digit exponent.
8	IN SYNC	LED lights when sync is acquired automatically and then synchronized.
9	SYNC LOST	LED lights when, at any time during a measurement, sync is lost.
10	MODE	Illuminated button is used to select CLOCK FREQUENCY, TOTAL ERRORS, ERROR RATE AUTO, and ERROR RATE MANUAL postions as required.
11 12	MANUAL RANGE EXPONENT SELECT	Two illuminated buttons light when the MODE button is pushed continuously until the BIT ERROR RATE MANUAL RANGE indicator lights. Push the upper MANUAL RANGE EXPONENT SELECT button to increase the exponent indicated on the display, or push the lower button to decrease it, until the desired range of from 10^{-2} to 10^{-9} is selected.
13	RESET	Illuminated button is used to help display TOTAL ERRORS, to stop error measurement, and to reset the display to zero while in HOLD time so that a new measurement can be initiated.

14	DISPLAY TIME	Vertical three-position slide switch selects three different display times: 1 SEC, 10 SEC or HOLD.
15	BIT ERRORS/ ECL	BNC output connector indicates a one pulse per bit error, width follows clock input width, at ECL level of 0.8V into 50 ohms to -2V.
16	FRAME SYNC/ TTL	BNC output connector indicates a squarewave occurring once every 4 pseudorandom sequences or every four 16-bit fixed words.
17	AUTO/SELECT	Illuminated button automatically selects reference data and displays by means of REF DATA LEDs. Sync is also acquired automatically and a synchronized condition illuminates the IN SYNC LED.
18	MANUAL REF DATA/SELECT	Illuminated button lights when the AUTO button is pushed. This button must be continuously pushed until the MANUAL REF DATA SELECT button lights. Push the MANUAL REF DATA SELECT button for the desired range (2^7-1 PN thru 2^{23}-1 PN, or 16-BIT word).
19	MANUAL SYNC/ SELECT	Illuminated button lights when AUTO button is pushed. This button must be continuously pushed until the MANUAL SYNC button lights. Push the MANUAL SYNC button to synchronize; a synchronized condition illuminates the IN SYNC LED.
20	EXT COMMAND/ SELECT	Illuminated button lights when the AUTO button is pushed. This button must be continuously pushed until the EXT COMMAND button lights. Same as MANUAL SYNC operation except sync attempt is initiated by a signal applied to the EXTERNAL COMMAND INPUT BNC connector.
21	EXT COMMAND INPUT/BURST MODE	BNC connector to connect to an external sync signal. The BURST MODE is used in conjunction with the AUTO button being pushed until the MANUAL REF DATA SELECT and EXT COMMAND buttons light. The EXT COMMAND button must be pushed in for the BURST MODE operation to function.
22	Data	BNC connector indicates a choice of coupling (TMI, ECL or AC).
23	Clock	BNC connector indicates a choice of coupling (TMI, ECL or AC).
24	EXTERNAL REF DATA	BNC connector input for a 1kHz to 325MHz, ECL level of 0.8V into 50 ohms to -2V signal. This input must be externally aligned bit-by-bit, with the data input.

25	CLOCK Input Level	Vertical three-position slide switch indicates a sinewave or square-wave in a choice of coupling (TMI, ECL or AC). The AC, TMI inputs range from 1kHz to 325MHz with 1V into 50 ohms to ground; AC and DC coupled respectively. The ECL input ranges from 1kHz to 325MHz with 0.8V into 50 ohms to -2V, DC coupled. An LED indicates when clock input is detected.
26	DATA Input Level	Vertical three-position slide switch indicates a choice of coupling (TMI, ECL or AC). The AC, TMI inputs range from 1kHz to 325MHz with 1V into 50 ohms to ground; AC and DC coupled respectively. The ECL input ranges from 1kHz to 325MHz with 0.8V into 50 ohms to -2V, DC coupled. An LED indicates when the data are all zeros (not present).
27	PHASE	Horizontal three-position slide switch selects additional three steps of delay input data relative to clock for proper clock/data phasing, approximately 3ns maximum delay.
28	ALL ZERO INPUT DATA	LED lights when data are all zeros (not present).
29	CLOCK ON	LED lights when clock signal is present.
30	EXTERNAL DATA	LED lights when the AUTO button is pushed. This button must be continuously pushed until the EXTERNAL DATA LED lights.
31	16-BIT WORD	LED lights when the MANUAL REF DATA SELECT button is pushed for 16-BIT WORD.
32	Pseudorandom Sequence	LED Lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{23}-1.
33	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{20}-1.
34	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{15}-1.
35	Pseudorandom Sequence	LED lights when the MANUAL REF DATA SELECT button is pushed for pseudorandom sequence of 2^{7}-1.

5.5 OPERATION

5.5.1 SYSTEM UNDER TEST CONNECTION

The MB-302 requires a clock and data signal, both at the same rate, in order to synchronize and perform error measurements. These connections must be made with a 50-ohm coaxial cable using BNC connectors.

5.5.2 INPUT LEVEL SELECT

The front-panel CLOCK and DATA input levels must be selected prior to starting the test. The TMI and ECL signals are DC coupled 50-ohm inputs with the reference termination voltage at ground and -2V, respectively. The AC input is a capacitively coupled 50-ohm input impedance.

5.5.3 REFERENCE DATA SYNCHRONIZATION MODES

There are five modes of synchronization possible with the MB-302, the modes are chosen by the SELECT pushbutton, which is also the AUTO mode LED, in the REF DATA/SYNC section of the front panel. Each time this SELECT button is pushed, the appropriate LED should light which shows the selected mode.

5.5.3.1 AUTO

In this mode, the MB-302 Reference Data is automatically selected to match the incoming data at the front panel. In addition, synchronization is acquired automatically once the receiver has determined the correct pattern. If, at any time during the measurement, synchronization is lost, the SYNC LOST LED will light; the receiver will automatically initiate a resynchronization sequence and, if synchronization is reacquired, both the IN SYNC and SYNC LOST LEDs will be on. The RESET pushbutton will extinguish the SYNC LOST LED.

5.5.3.2 MANUAL REF DATA SELECT/MANUAL SYNC

When this mode is chosen, via the SELECT pushbutton, both of these LEDs will light. Push the MANUAL REF DATA SELECT button and watch the REF DATA LEDs, in the upper left-hand corner, sequence through the patterns until the REF DATA pattern agrees with the MN-302 pattern.

Once the patterns are matched, push the MANUAL SYNC, if the input data error-rate is within the acquisition threshold, the IN SYNC LED should light, observe the error display in either of the bit error-rate modes or totalize, adjust the PHASE switch to minimize the error count.

If the receiver loses synchronization due to high error-rate at the data input, the SYNC LOST LED will be ON and the IN SYNC LED will be OFF, the only way to re-establish sync acquisition is to push the MANUAL SYNC button.

NOTE: This may happen when adjusting the PHASE switch during initial set-up of the system.

5.5.3.3 MANUAL REF DATA SELECT/EXT COMMAND

This mode functions similar to the MANUAL REF DATA SELECT/MANUAL SYNC mode except that the initiation of the sync acquisition function is done with an externally applied TTL pulse. Push the SELECT button until the MANUAL REF DATA SELECT and EXT COMMAND LEDs are lit. Check that the EXT COMMAND button is in the OUT (unlatched) position. Connect the external command signal source to the EXTERNAL COMMAND input, the signal is active LOW and synchronization is initiated on the LOW to HIGH transition (trailing edge) of this signal. This signal is TTL into the 1k-ohm input level, the minimum width is 50ns.

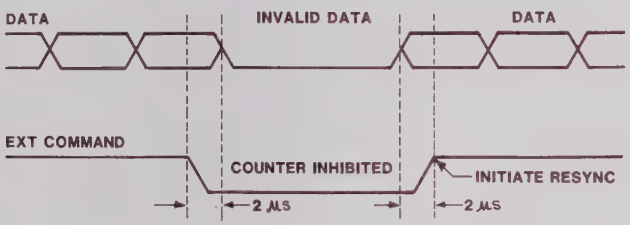
If receiver synchronization is lost then the EXT COMMAND pulse must be applied in order to re-establish the IN SYNC condition.

5.5.3.4 MANUAL REF DATA SELECT/BURST MODE

Push the select pushbutton until the MANUAL REF DATA SELECT/ EXT COMMAND LEDs light, then push the EXT COMMAND button so that it latches. Select the REF DATA PATTERN by pushing the MANUAL REF DATA SELECT pushbutton and observing the REF DATA LEDs in the upper left-hand corner of the front panel. In this mode, two operations take place, when the EXT COMMAND goes from its normal logic-1 value to logic-0, the MB-302 Error Counter is inhibited for the duration of the logic-0 level; when the EXT COMMAND makes a logic-0 to logic-1 transition, the synchronization process is initiated and resynchronization acquisition will occur.

This mode is used when the data are present in bursts or when continuous data have bursts of nonvalid data; in either case, error counting can be enabled only when the data are ready for measurement.

NOTE: The IN SYNC and SYNC LOST LEDs may be on simultaneously during a test in the BURST MODE because, even though the error counters are inhibited, the error threshold circuits are still active. The actual EXT COMMAND signal should have some guard band of approximately 2 micro-seconds on either side of the burst pulse to allow for loss of sync and reacquisition of sync before the counters are enabled.

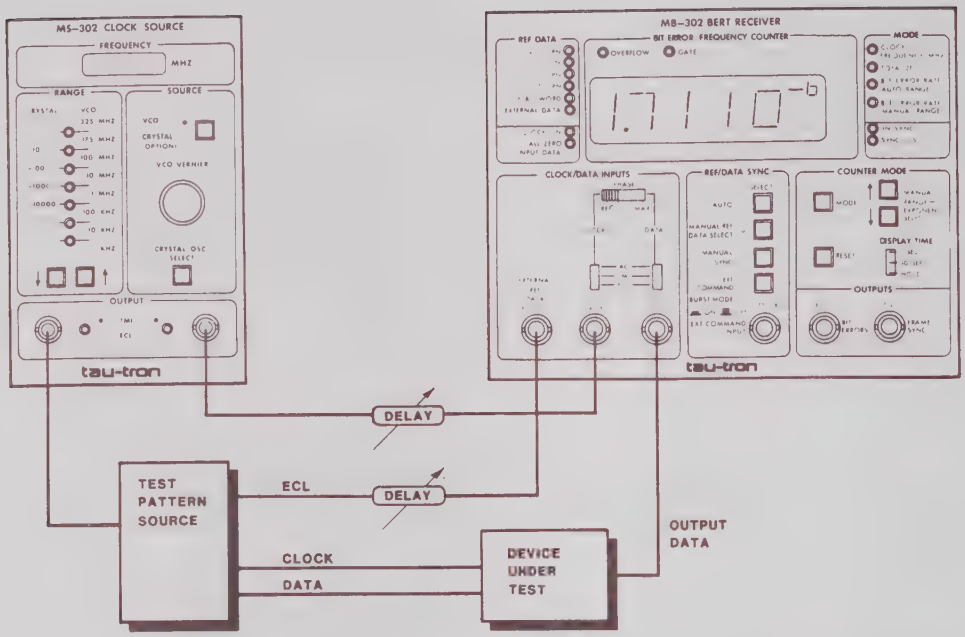


BURST MODE TIMING DIAGRAM

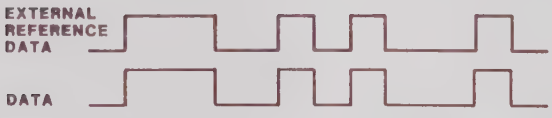
5.5.3.5 EXTERNAL REF DATA

In this mode, the MB-302 functions as a 2-channel comparator and any two identical data streams can be used as the input. Push the SELECT button until the MANUAL REF DATA SELECT LED is lit, then push the button again until EXTERNAL DATA is selected on the REF DATA indicators. Refer to page 5-12 for Test and Timing Diagrams.

Connect the MB-302 EXTERNAL REF DATA input to an output of the test pattern source via a 50-ohm coaxial cable and a variable delay control. (Note that the MB-302 EXTERNAL REF DATA input must be ECL, the input termination is 50 ohms to -2 volts.)

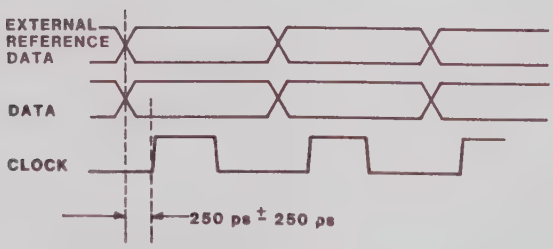


EXTERNAL REFERENCE DATA TEST DIAGRAM



BIT-BY-BIT ALIGNMENT

FINE TUNED DATA ALIGNMENT



DATA/CLOCK TIMING

EXTERNAL REFERENCE DATA TIMING DIAGRAMS

Connect the Device Under Test (DUT) output to the MB-302 DATA input. Make the appropriate input level selection. Set the MB-302 CLOCK/DATA PHASE control to the REF position.

Connect the MN-302 CLOCK input to the system clock output via a 50-ohm cable and a variable delay control.

Observe the EXTERNAL REF DATA input and the DATA input on a dual channel oscilloscope with matched delay inputs. Adjust the REF DATA variable delay control until it agrees with the DATA input bit-for-bit, then fine tune the delay control until the edges of the two data inputs are aligned to within ±100 pico-seconds.

Observe one of the DATA inputs and the CLOCK inputs, adjust the clock delay for the timing as shown in the diagram. Connect all inputs to the MB-302, fine tune the clock phase to minimize the error display. (ZERO errors if the set-up is using error-free data.)

Push the RESET pushbutton to initialize the counter and begin the test. The following characteristics of this mode should be noted:

1. There is no "synchronization/acquisition" function in the mode; hence, the IN SYNC/SYNC LOST LEDs have no meaning when determining the sync status.
2. The error counters function in all modes as before, the SYNC LOST LED may serve as a coarse indicator of burst error conditions, but as just mentioned, there is no "sync acquisition" function.
3. If large changes are made to the clock frequency, then all input timing must be rechecked.
4. The CLOCK/DATA PHASE control must NOT be moved from the REF postion.

5.5.4 COUNTER MODES

Four measurement modes are possible; all are selected by the MODE pushbutton in the COUNTER MODE section of the front panel.

CLOCK FREQUENCY — Push the MODE button until the CLOCK FREQUENCY LED lights. The display indicates the frequency in MHz, up to 6 digits plus overflow, with a 1kHz resolution. The GATE LED lights while the measurement is in progress.

TOTAL ERRORS — Push the MODE button until the TOTALIZE LED lights. The display indicates the number of total errors accumulated after the RESET button is pushed, up to 6 digits plus overflow. The GATE LED lights while the measurement is in progress. The measurement is stopped by pushing the RESET button.

ERROR RATE AUTO — Push the MODE button until the BIT ERROR RATE AUTO RANGE LED lights. In this mode, the range is selected automatically for 10^{-2} to 10^{-9}. The display indicates the error-rate, up to 3 digits plus overflow, with a 2-digit exponent. The GATE LED lights while the measurement is in progress.

ERROR RATE MANUAL — Push the MODE button until the BIT ERROR RATE MANUAL RANGE LED lights and the two MANUAL RANGE EXPONENT SELECT buttons light. Push the upper MANUAL RANGE EXPONENT SELECT button to increase the exponent as indicated on the display, or push the lower button to decrease it, until the desired range of from 10^{-2} to 10^{-9} is selected. The display indicates the error-rate, up to 3 digits plus overflow, with a 2-digit exponent. The GATE LED lights while the measurement is in progress.

NOTE: In the ERROR RATE modes (AUTO or MANUAL) the error-rate measurement is not valid until the END of the gate period, at this point the GATE LED goes out and the display is updated with the final count value.

5.5.5 DISPLAY TIME

Three different times are possible, all are selected by the DISPLAY TIME switch: 1 sec, 10 SEC or HOLD. With the 1 SEC or 10 SEC times, the display is held for the indicated time, then both the measurement and display are automatically reset to zero and a new measurement is initiated. With the HOLD time, the display is held until the RESET button is pushed at which time the display resets to zero and a new measurement is initiated.

NOTE: The BIT ERRORS output produces a pulse at an ECL level each time an error is detected during measurement, independent of the measurement mode selected. This output would be connected to an external counter so as to count total errors while the MB-302 is measuring the error-rate. As a result of this, a simultaneous indication of total errors and error-rate would be produced.

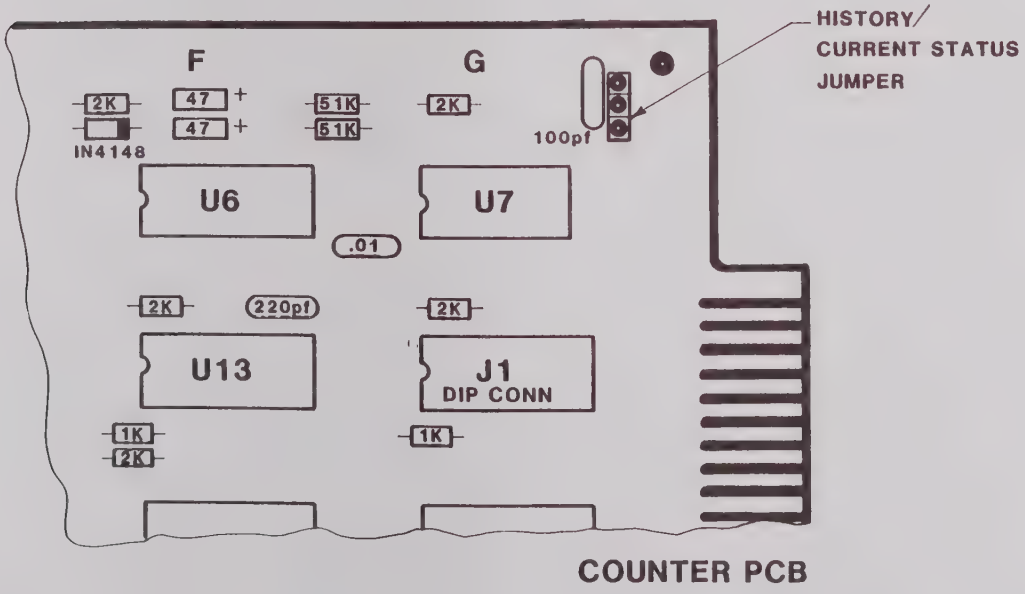
5.5.6. PRINTER INTERFACE

The MB-302 Printer Interface connector on the MF-5 Mainframe rear panel has all the available handshaking necessary to interface to any standard parallel BCD printer. Lines include 6 BCD digits plus decimal point, printer strobe, printer busy input, and status lines for time rate auto, time rate manual, frequency, totalize, in sync and lost sync.

NOTE: Ensure that the internal cable in the MF-5 Mainframe lines up correctly with the MB-302 Printer Interface connector.

5.5.6.1 CURRENT STATUS VS HISTORY STATUS

When in the current status mode and a BCD printer interface is installed in the system, the system will print twice for every over-threshold measurement or for every measurement the system takes. If this is undersirable, switch over from the current to the history mode by changing the jumper on the Counter PCB. This, as a result, lets the system update and print only once for every measurement.



COUNTER PCB

5.6 THEORY OF OPERATION

The MB-302 receiver (refer to the system Block Diagram) performs bit-by-bit measurements between incoming data and its own locally generated reference generator. Bit errors exist when the incoming data and the reference generator do not agree on a bit-by-bit basis. The bit errors are then displayed in a variety of ways to the user; one is totalize where all errors from the start to the end of a test are accumulated, another is automatic time rate where the errors are displayed as a function of the total number of bits in the measurement internal. In this mode, the exponent is automatically selected as a function of the number of errors. The third way is manual bit error-rate where the gate time interval can be set manually with a front-panel pushbutton. An overflow LED signals when the measured errors exceed the range of the selected time interval or the six-digit totalize range.

The MB-302 contains a front-panel board which holds the high-speed input amplifiers, a Code Resync board where the reference pattern generator, frame sync circuits, and error detectors are located and a Counter board which contains all of the error counting logic and sync acquisition control functions. Standard units contain a BCD Interface board for the Printer Output. If GPIB option is installed, the BCD Interface is replaced by the GPIB Interface board.

5.6.1 FRONT-PANEL BOARD

The front-panel pc board contains the high-speed clock and data input amplifiers as well as the display and display control logic.

5.6.1.1 INPUT CLOCK AND DATA AMPLIFIERS

Identical wide-band, pulse amplifiers convert the three selectable input signals to ECL for use within the module. An internal threshold adjustment is factory-set for maximum sensitivity and frequency response. These amplifiers, designed by Tau-Tron, are plug-in hybrid micro-circuits and operate as extremely fast current-mode switches. Output rise and fall times are typically much less than one nano-second when driving 50-ohm terminated lines.

5.6.1.2 6-DIGIT DISPLAY

The 6-digit LED display is driven from a display controller/driver mounted on the front panel. The display controller multiplexes data from the counter board and, under control from an oscillator on the counter board, presents the information to the display in the form of a scan across the six LED digits. The scan rate is such

that the indicators appear to be on continuously, but are actually on only when selected by the controller.

5.6.1.3 STATUS, REF DATA, AND OTHER INDICATORS

These single LEDs are driven from logic circuits or discrete component drivers and are essentially DC levels which reflect the status of the indicated signal as opposed to the digit LEDs which are dynamically driven.

5.6.2 CODE RESYNC BOARD

This board contains all of the reference pattern generator circuits and high-speed comparators which determine the bit errors. The circuit elements are ECL devices either in dual inline or flat-pack packages.

5.6.2.1 CLOCK DISTRIBUTION

The full-rate clock, from the input amplifier, drives a divide-by-2 circuit and this half-rate clock becomes the primary clock signal for the Code ReSync Board. The only places where the full-rate clock is used are at the input data latch and the error sampler. All other code generator processing is done at half rate.

5.6.2.2 REFERENCE PATTERN GENERATOR

The pattern generator itself is a variable length linear feedback shift register with feedback taps chosen such that the output is a maximal-length pseudorandom sequence. The pattern generator runs at half the input clock rate, but two phases are developed as input to the error detector so as to match the two phases of input data from the input data demultiplexer. The length of the shift register can be either 7, 15, 20 or 23 stages.

5.6.2.3 INPUT DATA LATCH AND DEMULTIPLEXER

A high-speed data latch, clocked at the input clock rate, transfers the input data to the data demultiplexer. The variable delay, under control of the front-panel CLOCK/DATA PHASE switch, insures that the transitions of the data with respect to the rising edge of the clock do not violate the setup time of the data latch. The demultiplexer translates the input data from a single data stream at the input clock rate to a pair of identical data streams at half the clock rate. These data streams are displaced by a 1/2 frame ±1 bit with respect to each other. In addition, these data streams along with the reference generator signals with identical frame phase relationships become the inputs to the Error Detector.

5.6.2.4 ERROR DETECTOR

The error detector is a network consisting of a pair of Exclusive-OR gates; each gate has a reference data bit stream and a demultiplexed input data bit stream as an input. Hence, although the processing is done at one half of the input clock rate, the use of two comparators insures that every input data bit, on a bit-by-bit basis, is checked against the reference code. The error detector output is an NRZ pulse for each data bit in error.

5.6.2.5 ERROR SAMPLER

The error sampler combines the two half-rate NRZ error channels from the error detector into a single high-speed error signal. To do this, the full-rate system clock strobes the two error channels such that every error bit is present as a pulse at the output. This error signal drives a buffer gate to the front-panel ECL BIT ERROR output jack. It also is the input to the Error Threshold counter section.

5.6.2.6 FRAME SYNC COUNTER

In order to generate a sync pulse on a per frame basis, the Frame Sync Counter detects a unique bit pattern within the frame period of the selected code. This unique pattern is the maximum number of consecutive zeros which, in this type of pattern generator, is always one less than the number of stages in the shift registor. For instance, in the 2^7-1 code length, there are seven stages in the shift register; therefore, six consecutive zeros occur, but occur only once in the 127-bit frame length. The same analysis holds true for the remaining code lengths except that the number of bits per frame and; hence, the time between frames, is considerably longer.

5.6.2.7 ALL ZERO DETECT

The absence of data of the MB-302 DATA INPUT will cause the ALL ZERO INPUT DATA LED to light. This signal is derived by sampling both phases of the demultiplexed input data and the most significant bit of the Frame Sync Counter. Under normal conditions, there will always be activity on the input data line and; hence, the zero indicators will not light. If the data are removed, then no activity is present on the input line, the receiver loses synchronization and the zero indicator will be set by the first transition out of the Frame Sync Counter most significant bit.

NOTE: It must be remembered, when in the AUTO SYNC MODE, that the absence of data (logic-0 at the input) or a continuous logic-1 at the input can cause a

condition where the system appears to be in sync even though there are no data present. This is because, in the AUTO SYNC mode, the static levels of logic-1 or 0 are interpreted as a 16-bit fixed word and; hence, represent a valid data pattern even though the original pattern may have been one of the pseudorandom codes.

5.6.2.8 HIGH-SPEED ERROR COUNTER

The first stage of error counting, which corresponds to the least significant digit on the error display, is done on the code ReSync Board. The input to this first counting stage can be as high as 325Mb/s; hence, in order to localize the high-speed signals, a bi-quinary divider is used to count the first digit in both the bit error-rate and totalize count modes. The first stage of error counting for the threshold circuits is also done on this board, sharing logic circuits with the totalize counting circuits. Two error count signals are sent to the Counter Board from the Code Resync Board, one is the E/4 signal to the threshold logic and the other is the least significant digit (BCD) for the display. In addition, a CLOCK/20 is also generated on the ReSync Board for use on the Counter Board.

5.6.3 COUNTER BOARD

The Counter Board accepts the error signals and prescaled clock signals from the ReSync Board and generates all of the error display information for the front panel. In addition, the digital error threshold circuits are located on this board; these circuits determine whether the amount of bit measured errors with respect to the number of bits sampled exceeds a pre-defined ratio.

5.6.3.1 ERROR THRESHOLD

The error threshold logic has two thresholds for operation, a low threshold which is active when the receiver is trying to establish code synchronization (search) and a high threshold which allows the receiver to maintain code synchronization in high error-rate situations (hold). The thresholds are as follows:

MODE	SEARCH (LOW) THRESHOLD	HOLD-IN (HIGH) THRESHOLD
P/N SEQUENCE	64 errors/800 bits	3200 errors/10,000 bits
FIXED WORD	32 errors/1600 bits	1600 errors/10,000 bits

The thresholds are determined by fixed dividers on the system clock which provide the block of bits over which the error measurement must be made, the high-speed

dividers on the ReSync board provide the error information to the low-speed counters on the Counter Board. The block of bits determines an error threshold frame which resets the error accumulators at the end of the block time. If the accumulator is filled before the end of the frame, then an over-threshold condition exists and other circuit and system functions are initiated.

5.6.3.2 TIME BASE CONTROL AND COUNTER

The Time Base Counter is an 8-decade counter driven by a pre-scaled clock pulse from the Code ReSync board. The counting window or time base is selected by the Time Base Control which enables the proper decade. This decade is represented by the exponent on the front-panel display and may be selected manually or automatically. The range of the exponent is from 10^{-2} to 10^{-9} which selects decade divider ranges from 10^{-4} to 10^{-11}.

5.6.3.3 ERROR COUNTER

The actual error counter is a six-decade BCD counter; the least significant digit is located on the ReSync board and is a high-speed bi-quinary circuit, this output drives the remaining 5 decades on the counter board which are low-speed (TTL) BCD dividers. The counter outputs drive data selectors which control the multiplexing of the counter onto the scanned front-panel display.

5.6.3.4 DISPLAY TIME

The front-panel DISPLAY TIME switch controls the time constant of a TTL one-shot multivibrator. This circuit controls the rate at which the display holds its information for observation by the user. The display time generator also provides reset and preset signals to the error counters, time base counters and error latch circuits; these signals occur at the end of the display time.

5.6.4 THE SYNCHRONIZATION PROCESS

The synchronization of incoming data with the internal reference data is accomplished using a "feed-forward" technique. Assuming that the receiver is not synchronized with the incoming data, an output from the error threshold detector will cause the incoming data stream to be loaded into the internal reference code generator shift register. At the end of 800 bits, the feed-forward signal is removed and the reference generator begins to shift on its own, advancing to the next state of the code. The input data should also be advancing to the same state and; hence, the errors should be zero. The error detector compares the two data streams, one from the reference

generator and one from the device under test. If the errors are less than 64 over the next 800 bits, then the input data are assumed to be correct and the error threshold converts to the high threshold value where errors less than 3200 in 10,000 bits are required to maintain synchronization. This basic procedure is used in all sync modes and pattern selections.

5.6.4.1 AUTO SYNC MODE

In this mode, the search for the proper internal reference code is done automatically. Assuming initially that the receiver is not synchronized, the basic feed-forward procedure is initiated. If, at the end of an 800-bit sample, the error threshold is exceeded, then the procedure is re-initiated. If, after the second attempt, the error threshold is still too high, the reference code selector is automatically advanced to the next pattern and the synchronization procedure starts again. This will continue until all of the pattern lengths have been examined at least twice. This can be observed on the front panel, the REF DATA indicators will be flashing as they are selected.

5.6.4.2 MANUAL SYNC MODES

All of these modes require that the internal reference code be selected manually with the front-panel controls. The other common feature of the manual modes is that some external signal must generate the feed-forward or re-synchronization signal. In the MANUAL mode, it is the front-panel pushbutton and, in the EXTERNAL modes, it is from some other electrical signal. If synchronization is acquired and then lost, the external re-sync signal must be applied in order to start the synchronization process again.

5.6.5 THE COUNTING PROCESS

The counter section provides three methods of counting bit errors, two of them are bit error-rate modes and the third is a totalize mode. In addition to counting errors, the counter functions as a frequency meter and displays the input clock frequency on the front-panel display.

5.6.5.1 BIT ERROR RATE AUTO

In this mode, the exponent of the bit error-rate is automatically set as a function of the measured errors. The exponent always starts at 10^{-2} and increments to the next

lowest error-rate -- 10^{-3}, 10^{-4} etc. Each selection of an exponent enables an increased counting window in the error counter because the exponent is a direct function of the number of bits or clock periods over which the measurement is being taken. The exponent will continue to increment until a minimum of 200 errors are counted in a particular range. Once at least 200 errors are counted, the measurement will continue until the end of the counting window; at that time the exponent will be incremented to the next value and the display will be updated with the present value held in the error-counter buffer. The counters get reset and the count cycle re-starts at 10^{-2}, incrementing at the end of each exponent time-out until at least 200 errors are detected. If no errors are detected, the counter will reach 10^{-9} and remain there.

5.6.5.2 BIT ERROR RATE MANUAL

In this mode, the counting window is set via the front-panel EXPONENT SELECT push-buttons. The count window is fixed and errors are constantly measured over the same time base. If the errors exceed the time base, then an overflow condition exists, and the OVERFLOW LED will be lit. The overflow condition can be avoided by setting the exponent to some higher error-rate value.

NOTE: The GATE LED is illuminated during the time that the counter gate is open. The displayed value is valid only at the END of the count cycle when the GATE LED goes out and the counter is updated with the final value.

5.6.5.3 TOTALIZE

The totalize mode functions by opening the count gate at the start of a measurement (such as after a reset) and will not close the gate until the RESET button is pushed or the mode is switched. In this mode, errors accumulate indefinitely or until the measurement is deemed to be complete. If the six-digit counter overflows, the OVER-FLOW LED remains on while the overflow condition exists.

5.6.5.4 FREQUENCY

In the Frequency mode, the input clock frequency will be displayed on the front panel. The units displayed are Megahertz but the six-digit display has resolution down to 1 kilohertz. A 1MHz crystal time base divided down to 10^{-5} provides the basic counting window for this measurement. The 10 millisecond squarewave enables the input clock to be divided and entered into the display buffer. At the end of this time, the value is latched and presented to the display.

5.6.6 BCD INTERFACE

The BCD Interface is a synchronous demultiplexer with six output latch sets, one for each of the five data digits and one for the exponent digit. When the MB-302 gate signal goes low, indicating end of measurement, the BCD Interface starts looking for the first data byte address, 0. The interface then latches the data byte into the corresponding output data latch. When address 6 is detected, all data have been loaded and are ready for the printer where a print strobe is generated. When the printer responds with a $\overline{\text{BUSY}}$ signal, the BCD Interface holds the output data stable and does not accept any more data from the MB-302 until the printer $\overline{\text{BUSY}}$ line goes high, initializing the interface for the next block of data.

5.6.7 MODULE POWER SUPPLIES

The unregulated mainframe voltages of ±34 and ±17 are the inputs to voltage regulators located on the rear and side of the module. The +34V and -34V drive the +15V and -15V regulators with loads of much less than 1A. The +17V is regulated to +8V which provides power to the micro-circuit amplifiers and is also the input to a +5V regulator located on the clock source board. This voltage is used for TTL logic circuit power. The -17V is regulated to -5.2V high current supply using a combination of a three-terminal regulator and boost transistor. This voltage is also used to drive a pc board mounted -2V regulator which supplies the termination voltage for the high-speed ECL circuits.

5.7 GPIB OPTION

GENERAL

All front-panel controls, except CLOCK/DATA INPUTS PHASE and MANUAL SYNC switches, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An associated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired. This option replaces the standard printer output.

MESSAGE Format

The message consists of five digits (in ASCII code) followed by a terminator.

Ident	CNTR Mode	SYNC Mode	REF DATA	BER EXP	Termi-nator

Ident

Digit	Meaning
3	MB-302

CNTR Mode

Digit	Meaning
0	Bit error rate-Manual range
1	Bit error rate-Auto range
2	TOTALIZE
3	Clock frequency

SYNC Mode

Digit	Meaning	
0	Auto synchronization	
1	Manual synchronization	Burst
2	EXT COMMAND sync	mode
3	EXT REF DATA	enabled
4	Auto synchronization	
5	Manual synchronization	Burst
6	EXT COMMAND sync	mode
7	EXT REF DATA	disabled

Internal REF DATA

Digit	Meaning
0	2^7-1 pseudorandom pattern
1	2^{15}-1 pseudorandom pattern
2	2^{20}-1 pseudorandom pattern
3	2^{23}-1 pseudorandom pattern

Digit	Meaning
4	Any 16-bit pattern
5	Illegal
6	Illegal
7	Illegal

BER Exponent — Any number in ASCII code between 2 and 9 inclusive.

Terminator — Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

Measurement Output — Place the MF-5 in TALK mode following GPIB protocol. The MF-5 will now send measurement and status data back to the GPIB controller when available. No prior module ID setup is necessary since the MF-5 interface will support only one GPIB talker module. Whenever a measurement is available, the MB-302 will load the measurement value and status bits into the MF-5 GPIB interface. If addressed to talk, the MF-5 GPIB interface will immediately send an 11-character (ASCII code) message containing a space between the status digit and measurement (including overflow) digits, followed by the terminators CR and LF.

STATUS DIGIT	SPACE	OVER-FLOW DIGIT	MSD	2nd	3rd	4th	5th	LSD	CR	LF

Definition of the digits are as follows:

STATUS DIGIT:

ASCII DIGIT	SYNC LOST	IN SYNC
0	FALSE	FALSE
1	FALSE	TRUE
2	TRUE	FALSE
3	TRUE	TRUE
+	FREQUENCY MEASUREMENT	
OTHER VALUES	ILLEGAL	

OVERFLOW DIGIT:

+	OVERFLOW TRUE
SPACE	OVERFLOW FALSE

MSD THRU LSD:

Decimal numbers, period, or minus sign

MEASUREMENT	FORMAT (MSD FIRST)
BIT ERROR RATE	A . BC - D
TOTALIZE	A B C D E F
FREQUENCY	A B C D E F (in kHz)

Measurements become available at the end of the measurement gating period. This happens automatically in all counter modes except TOTALIZE. For a TOTALIZE measurement, the gating period is infinite; thus, the MB-302 will not automatically generate a measurement output. The controller can request the current total error measurement by issuing a group execute trigger (GET) while the MF-5 is addressed to LISTEN. A service request will be generated if enabled.

Service Request Serial Poll

When the MB-302 has a measurement available, and the MF-5 is not addressed to talk, a service request ($\overline{SRQ}$) will be generated if the SRQ INHIBIT switch on the rear panel of the MF-5 has not been set. This alerts the controller that a device on the bus needs service. The normal controller response would be a serial poll to determine which device needs service. When serial polled, the MF-5 will respond with 41 (hexadecimal) to indicate that it needs service. If the MF-5 does not need service it responds with 00 (hexadecimal).

When power is first turned on, the $\overline{SRQ}$ interrupt will normally be present if enabled at the rear of the MF-5 Mainframe. In the bit error-rate or frequency mode, this is caused by the termination of the first measurement. In the totalized mode the interface card and the MF-5 will load the data present at its input into its buffer. When power is turned on, the mainframe rear-panel RESET button should be pushed. $\overline{SRQ}$ may be cleared by issuing an IFC in bit error-rate or frequency modes. Of course, SRQ will be set again when the next measurement is completed. In the totalized mode the only way to clear the $\overline{SRQ}$ interrupt line is to address the MF-5 as a talker and turn off the ATN signal. No actual data transfer need take place, unless desired.

DISPLAY TIME Control

The DISPLAY TIME control, along with the other slide switches on the front panel of the MB-302, is not under remote/local control. All slide switches are always under local control. Care should be taken to see that the DISPLAY TIME control is set to either 1 second or 10 seconds when the MB-302 is under GPIB control. If the DISPLAY TIME control is set to hold, the MB-302 will not make continuous outputs to the GPIB controller. Measurements will stop after 1 measurement is taken, unless the GPIB controller issues a DCL or SDC bus command to initiate another measurement.

Manual Synchronization

When the GPIB controller places the MB-302 into the manual synchronization mode, it cannot initiate a manual synchronization attempt. This can only be done by pushing the front-panel MANUAL SYNC pushbutton, which is always active: independent of the remote/local mode.

Burst Mode

In local operation, the burst mode is indicated by the position of the external command pushbutton. Under GPIB control, the controller can place the MB-302 into either the burst or the non-burst mode. However, there is no way to indicate which mode has been selected on the front-panel of the MB-302 since the physical position of the external command pushbutton does not reflect the GPIB setting.

Manual Bit Error Rate

When the manual range-bit error-rate is selected by the GPIB controller, it can also select the exponent. The exponent will always be found by an automatic incrementation of the current exponent until it equals the exponent selected. The front-panel "up" exponent pushbutton is also disabled, but would interfere with the exponent selection if held. Therefore, when under GPIB control, do not push the front-panel "down" exponent select pushbutton.

Automatic Synchronization

When under local control, automatic synchronization also means automatic pattern selection. When under GPIB control, automatic synchronization does not mean automatic pattern selection. Pattern auto/synchronization selection under GPIB control is auto/synchronization only, not auto/pattern selection.

Changing Measurement Modes

When changing modes to make a new measurement, a sync or overflow error will occur. This is due to the previous measurement data being held in the output latch of the interface card.

GPIB Interface Card prior to serial number 8301001

A measurement is almost always held in the software buffer, even after the hardware buffer (earlier version), has been cleared (per above). Consequently, in order to clear the buffer, an additional measurement of the previous mode must be accepted after the COUNTER MODE has been changed on the MB-302. This is especially true when changing from the FREQUENCY MODE to another mode; i.e., it becomes necessary to accept an additional frequency measurement whenever a FREQUENCY MODE change is made.

In the TOTALIZED MODE, however, a measurement will not usually be waiting in the software buffer unless commanded by a GET command, and not serviced. That is, measurement entry into the software buffer is to be under user control via the GET command. Therefore, it is up to the user to determine from his controller software, whether or not he has serviced the last commanded totalize transfer before changing to the COUNTER MODE. If he has, there will not be any totalize measurement in the buffer after the COUNTER MODE has been changed.

Similarly, when changing from either of the bit error rate modes to another mode, the IFC clears the output registers. When the MTA is true, then the buffers are loaded, and placed on the output bus.

5.8 SERVICE

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

5.8.1 ROUTINE SERVICE

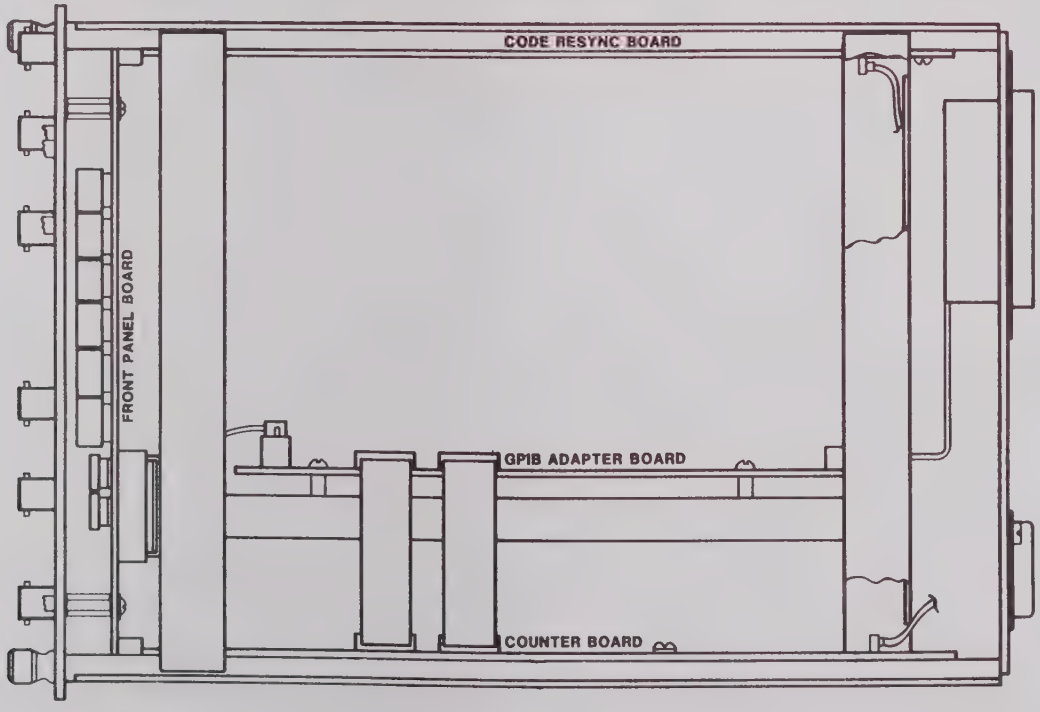
Routine service includes the performance of checks and service procedures which prevent or minimize the downtime of the unit. The checks and service are simplified, and may be limited to visual inspection for defective components, loose hardware and/or accumulation of dust within the unit at critical areas.

NOTE: It is recommended that periodic cleaning (approximately once every three months) of the interior and exterior of the unit be done with a vacuum cleaner.

Refer to Section 5.3, INSTALLATION, for module removal.

Board Seating

Ensure that all printed cicuit boards are securely seated in their connectors as shown in the illustration below.



MB-302

5.8.2 REPAIR RETURNS

For mechanical damage or electrical malfunctions, refer to Page ii, REPAIR RETURNS.

5.8.3 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617) 256-9013. Their experience and expertise can often save you valuable time in correcting any equipment malfunction.

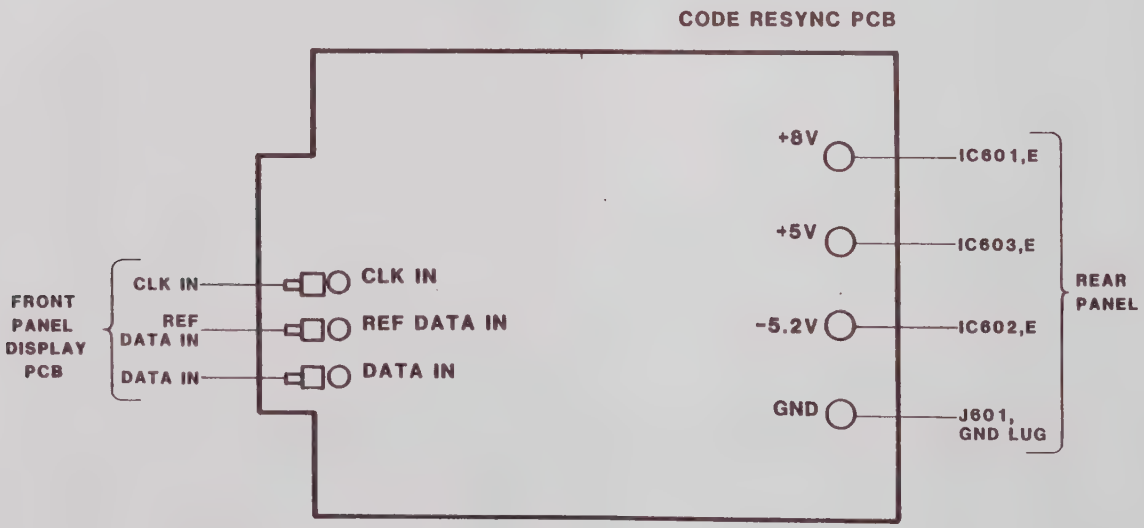
5.8.4 TROUBLE ANALYSIS

DANGER: Hazardous voltages exist in this equipment. Do not attempt access to the interior without first disconnecting the line cord from the power receptacle to the MF-5 Mainframe.

DC Voltages

WARNING: While measuring the -5.2V DC power supply, ensure that utmost care is taken. A power supply could be either severely damaged or completely destroyed if it is accidentally shorted to ground.

Verify that the DC votages are correct by measuring them on the Code Resync circuit board. Refer to the illustration below for the proper measurement points.



If the correct voltages are not indicated, consult the factory.

Calibration

Routine calibration is not normally required except in the following situations:

a. Failed component or circuit. Consult factory for further details.

b. Harsh environment; typical environment is:

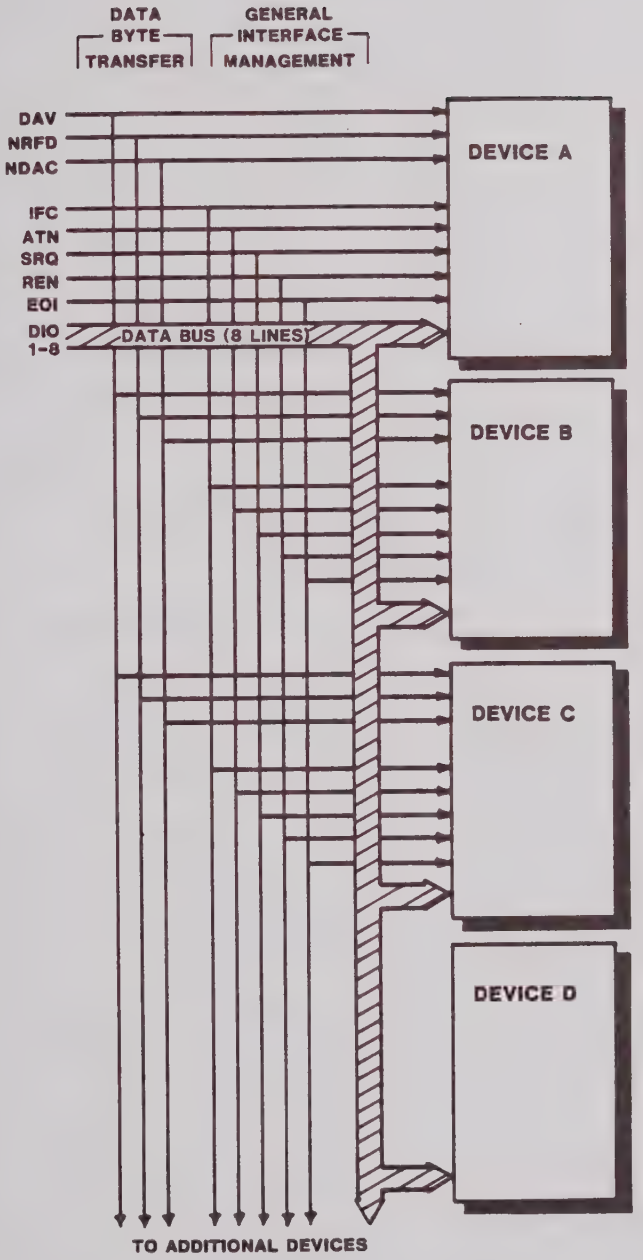
Temperature	32 to 95°F (0 to 35°C)
Humidity	0 to 95% RH max at 20°C, non-condensing.

Any calibrations or technical adjustments other than the situations mentioned above should not be made during the Warranty period unless otherwise authorized. Consult factory for further details. (Refer to sections 5.2 and 5.5, SPECIFICATIONS and OPERATION, respectively, for proper switch, control, level and LED indicator settings.)

6. GPIB OPERATION

6.1 DESCRIPTION

The GPIB (General Purpose Interface Bus) transfers data and commands between the units of an instrumentation system on 16 lines. The device functions for each unit are performed within the unit so only passive cabling is necessary to connect the system. The cables connect all instruments, controllers, and other units of the system in parallel across the signal lines.



Eight of the lines (DIO1 through DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer are asynchronous and coordinated by the three handshake lines: DAV (data valid), NRFD (not ready for data), and NDAC (not data accepted). The other five lines are for control of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the roll of each of the other units by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO1 through DIO8). Addresses are set into each device at the time of system configuration either by switches built into the unit or by jumpers on a printed-circuit board. While the ATN line is true, all units must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously, but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers should be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as units can respond, but no faster than allowed by the slowest device being addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII code. When ATN is false, any code of eight bits or less understood by both the talker and listener(s) can be used.

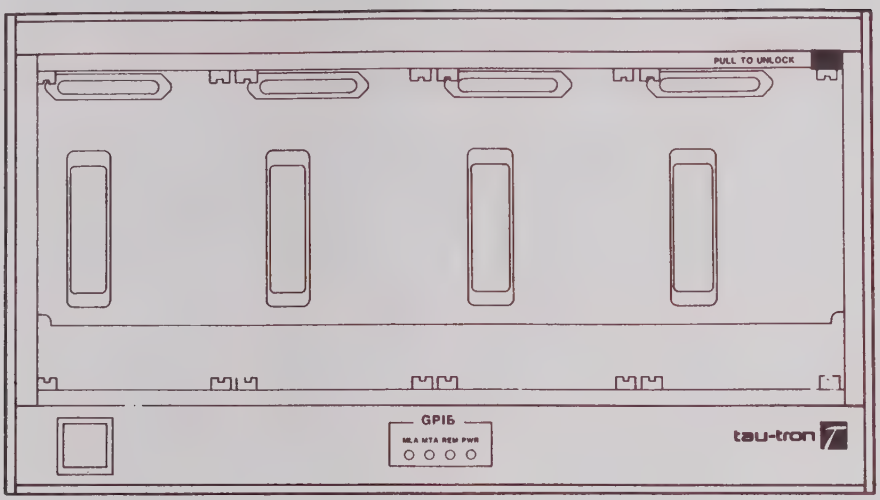
The other control lines are IFC, REN, SRQ, and EOI. IFC resets the handshake logic, MLA, and MTA only. No reset pulse is generated. REN (remote enable) is used with other coded messages to select either local or remote control of each unit.

Any active unit can set the SRQ (service request) line to true. This indicates to the controller that some unit on the bus wants attention; for example, a counter on a bus may want attention because it has just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (end or identify) is used by a unit to indicate the end of a multiple-byte transfer sequence. When a controller sets both ATN and EOI lines to true, each unit capable of a parallel poll indicates its current status on the data line (DIO1 through DIO8) assigned to it.

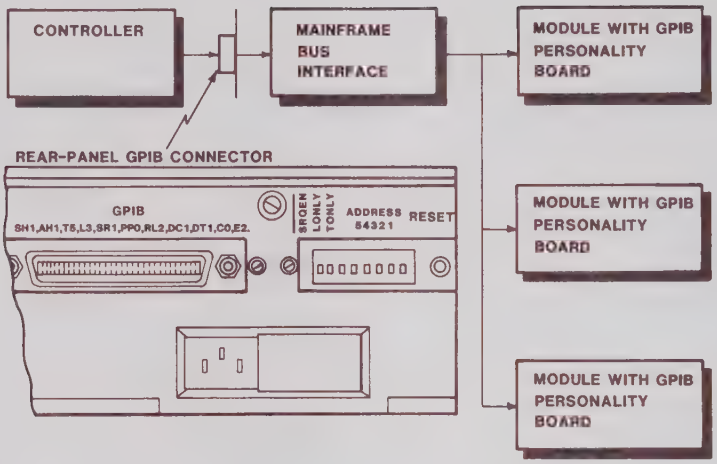
It is not necessary that every unit be capable of responding to all of the lines. Each unit can be designed to respond only to those lines that are pertinent to its functions on the bus.

6.2 MF-5 FRONT PANEL (GPIB)



1. MLA — My Listen Address indicator, lights when the, MF-5 Mainframe has been addressed to listen.
2. MTA — My Talk Address indicator, lights when the, MF-5 Mainframe has been addressed to talk.
3. REM — Remote indicator, lights when GPIB bus is in remote mode.
4. PWR — Power indicator, lights when power is present and the GPIB Interface in the MF-5 Mainframe has passed its power-on self test.

6.3 MF-5 MAINFRAME REAR PANEL



1. GPIB Interface Connections — A 24-pin GPIB connector is provided on the rear panel of the MF-5 Mainframe. Connector dimensions and pinouts correspond to IEEE-488 specifications.

2. GPIB Address and Option Selection — The 8-section DIP switch on the rear panel is used for GPIB talk/listen address and option selection as follows:

Switch	Function
8 (Left)	SRQ Enable..... With this switch down, the BERTS-325C is allowed to generate service requests (assert the GPIB SRQ line). Service requests can be inhibited by setting this switch up.

* Systems with serial numbers prior to 8301001 are set to operate in the opposite direction.

7....	Listen only.....	With this switch up, the BERTS-325C can be remotely controlled, but cannot be addressed to talk.
6....	Talk only.....	With this switch up, the BERTS-325C can transmit data, but cannot be addressed to listen (no remote control).
5....	Address A5(MSB)..	A1 thru A5 form the device talk and listen addresses; 0 through 30. Address 31, all switches up, is not valid.
4....	Address A4	
3....	Address A3	
2....	Address A2	
1....	Address A1(LSB)	

NOTE: The DIP switch is read on power-up only. To change the MF-5 Mainframe's GPIB address or other characteristics, push the RESET pushbutton alongside the DIP switch.

6.4 BERTS-325C GPIB CAPABILITIES

The BERTS-325C may be interfaced as a talker/listener, a talker only or a listener only. As described in the IEEE-488-1978 (GPIB) standard, the following GPIB capabilities are implemented:

SH1	Complete source handshake.
AH1	Complete acceptor handshake.
T5	Basic talker, serial poll, talk only, unaddress if addressed to listen.
L3	Basic listener, listen only, unaddress if addressed to talk.
SR1	Complete service request capability.
RL2	No local lockout on remote/local capability.
PP0	No parallel poll capability.
DC1	Complete device clear capability.
DT1	Complete device trigger capability.
C0	No control capability.
E2	Tri-state drivers are used.

6.4.1 RESPONSE TO GPIB COMMANDS

The following GPIB commands and events are responded to by the BERTS-325C:

Command	Function
GTL	Go to local.
SDC	Resets MB-302.
GET	Strobes Totalize on MB-302.
DCL	Resets MB-302.
SPE	Enables Serial Poll.
SPD	Disables Serial Poll.
MLA	Listen address as set by rear-panel switches.
MTA	Talk address as set by rear-panel switches.

Several GPIB capabilities are not supported by the BERTS-325C. The following commands are ignored by the BERTS-325C:

Command	Function
PPC	Parallel Poll Configure.
TCT	Take Control.
LLO	Local Lockout.
PPU	Parallel Poll Unconfigure.

6.5 MODULE I.D.

In order to control more than one module in a mainframe, the first digit of the LISTEN message is a module I.D. This directs the remaining digits of the message to only one module. To prevent spurious operation at power-on or during an IFC on the GPIB, Module I.D. 0 must not be used. The I.D. is selected by a jumper provision on the module personality card, so the I.D. number can be changed if a conflict does occur.

MODULE I.D. LIST

I.D. NO.	MODULE CATEGORY
0	Not Used
1	Clock Source (MS-302)
2	PR Generator (MN-302)
3	BERT Receiver (MB-302)
4	Data Generator
5	Code Conversion (MC-303/304)
6	Open
7	Open

6.5.1 SPECIFIC MODULES

For examples of applying to specific modules, see Sections 3., 4., and 5., GPIB Option.

NOTE: For module control, all four control digits need not be used (or transmitted). When the ICS card in the mainframe sees a terminator at the end of the message, it will transfer the digits to the MF bus.

7. PARTS

7.1 REPLACEABLE PARTS

This section contains a listing of all electronic components and mechanical parts subject to normal wearout or failure. In the index shown below, tables 7-1 through 7-3 are described. Each table references the replaceable parts according to Tau-Tron Part no., description and quantity required.

Table	Description	Page
7-1	MF-5 Mainframe	7-3
7-2	MS-302 Clock Source	7-16
7-3	MN-302 BERT Transmitter	7-26
7-4	MB-302 BERT Receiver	7-37

TABLE 7-1

MF-5

Mainframe

MFS CHASSIS ASSY GPIB

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0045	SCREW PNHD MET NC.4-40X3/8	4.000
8000-0047	SCREW PNHD MET NC.4-40X1/2	4.000
8000-0085	SCREW PNHD MET NC.6-32X3/8	3.000
8000-0087	SCREW PNHD MET NC.6-32X1/2	6.000
8000-0115	SCREW PNHD MET NC.8-32X3/8	11.000
8000-0802	SCREW SLF-TAP NO.4X1/2	6.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	2.000
8000-1005	NUT HEX MET NO.8-32	20.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
8000-1204	LOCKWASHER NO.6 INT TOOTH	25.000
8000-1205	LOCKWASHER NO.8 INT TOOTH	20.000
8000-9010	CLIP NUT TINNERMAN C195-832-4	8.000
8000-9014	SCREW MET HEXHEAD NO.8-32X1/2	8.000
8000-9037	CLIP NUT 8-32 TINNERMAN	8.000
9190-0010	FEET 25778D32	2.000
9190-0011	SWNG-OUT SIDE HANDLE B25778D26	2.000
9190-0014	BEZEL 25778D25	2.000
9190-0015	TORSION BAR 2577885	2.000
9190-0016	WELD STUD NO.8-32X5/8	16.000
9190-0018	TILT EALE 26217-3	1.000
9350-1001	PCB/RAIL GUIDE G3 35-1321A	16.000
9350-1006	SPACER STRIP 35-0482E	4.000
9350-1007	ID STRIP 41-1660J	1.000
9525-4477	MFS GPIB MOUNTING PANEL ASSY	1.000
9535-4603GPIB	CONN BRKT PWR & I/O ASSY GPIB	1.000
9585-4602	POWER SWITCH WIRING ASSY	1.000
9705-4301	EXTRUSION REWORKED	1.000
9705-4302	FRONT PANEL SUPPORT BRACKET	2.000
9705-4303	FRONT PANEL SUPPORT BRACKET	1.000
9705-4311L	LEFT SIDE PLATE REWRKD	1.000
9705-4311R	RIGHT SIDE PLATE REWRKD	1.000
9705-4312-1	EXTRUSION REWORKED	1.000
9705-4312-2	EXTRUSION REWORKED	1.000
9705-4315	AIR DEFLECTOR PLATE	1.000
9705-4321	LOCKING BAR ASSY REWORKED	1.000
9705-4467	FRONT PANEL BRACKET	1.000
9705-4485	BRACKET REAR PANEL TO FRAME	2.000
9705-4535	SHIM	2.000
9705-4558	SUPPORT BLOCK	2.000
9705-4575A	SIDE EXTRUSION FINISHED	4.000
9705-4575B	CORNER CASTING ASSY	4.000
9705-4575C	EXTRUSION TRANSVERSE FINISHED	2.000
9705-4575E	BOTTOM COVER FINISHED	1.000
9705-4575F	SIDE HANDLE RETAINER FINISHED	2.000
9705-4575G	SIDE COVER MODIFIED FINISHED	2.000
9705-4575H	CORNER INSERT FINISHED	4.000
9705-4575I	EXTRUSION REWORK-FINISHED	2.000

MF5 GPIB MOTHER BD PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-4300	RES COMP 3 KOHM 5P 1/2W	1.000
0272-2300	RES W.W. 30 OHM 10P 5W	2.000
1013-6710	CAP CER 1.0 MFD 10P 50V	1.000
1014-4610	CAP CER 0.1 MFD 20P 200V	1.000
1024-5110	CAP ELEC 1 MFD 35WVDC	1.000
2101-4001	DIODE RECTIFIER 1N4001	2.000
4200-340T5	IC LINEAR REGULATOR LM340T5	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	1.000
8000-1002	NUT HEX MET NO.4-40	1.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	1.000
8000-1302	FLAT WASHER MET NO.4	2.000
9100-0114	HEAT SINK TO-202 STYLE,60632	1.000
9300-0137	CONN EDGE 96POS RTAGL PCB MNT	1.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
9306-0047	CONN HDR 40POS RTAGL .125PCB	1.000
9318-0050	CONN RTAGL PC MNT 6 POS	1.000
96ART-54472	MF5 GPIB MOTHER BD PCB	1.000
96SCH-54471	MF5 GPIB MOTHER BD	1.000
9605-4472	MF5 GPIB MOTHER BD PCB	1.000

MFS MAINFRAME W/GPIB OPTION

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0117	SCREW PNHD MET NO.8-32X1/2	8.000
8000-0119	SCREW PNHD MET NO.8-32X5/8	8.000
8000-1205	LOCKWASHER NO.8 INT TOOTH	8.000
8000-1305	FLAT WASHER MET NO.8	8.000
8000-1413	FLAT WASHER NYLON NO.8	8.000
9525-4601	MFS REAR PANEL ASSY GPIB	1.000
9535-4600	MFS CHASSIS ASSY GPIB	1.000
9705-4575D	MFS TOP COVER FINISHED	1.000

MF5 REAR PANEL ASSY GPIB

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0032-4200	RES COMP 2 KOHM 5% 1/2W	4.000
1034-4545	CAP ELEC 45000 MFD 30WVDC	1.000
1035-5511	CAP ELEC 11000 MFD 40WVDC	3.000
2103-9902	DIODE RECTIFIER BRDG MDA990-2	2.000
8000-0023	SCREW PNHD MET NO.3-48X3/8	6.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	4.000
8000-0065	SCREW PNHD MET NO.6-32X3/8	24.000
8000-0525	SCREW PNHD NYLON NO.6-32X5/8	12.000
8000-0526	SCREW PNHD NYLON NO.6-32X3/4	2.000
8000-0695	SCREW FLTHD MET NO.10-32X1/4	8.000
8000-1001	NUT HEX MET NO.3-48	2.000
8000-1004	NUT HEX MET NO.6-32	28.000
8000-1005	NUT HEX MET NO.8-32	8.000
8000-1201	LOCKWASHER NO.3 INT TOOTH	6.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
8000-1204	LOCKWASHER NO.6 INT TOOTH	40.000
8000-1205	LOCKWASHER NO.8 INT TOOTH	8.000
8000-1206	LOCKWASHER NO.10 INT TOOTH	4.000
8000-1301	FLAT WASHER MET NO.3	6.000
8000-1306	FLAT WASHER MET NO.10	4.000
8000-1509	LUG SOLDER ANGLE NO.10	8.000
8000-1512	LUG SOLDER CLRNC NO.6	2.000
8000-9015	SCREW PNHD NO.10-24X1/2	4.000
8000-9016	NUT HEX MET NO.10-24 F/P DRESS	4.000
9000-0002	LINE FILTER 6J4	1.000
9000-0002A	CORCOM 6J4 .125 PANEL CLIP	2.000
9000-0053	AC LINE CORD	1.000
9000-0106	FUSE 3A SLO-BLO 3AG	1.000
9000-0252	FAN FILTER PAMOTOR 5502	2.000
9000-0253	FAN BRACKET SET PAMOTOR 5501	4.000
9000-0254	FAN SCREEN ASSY PAMOTOR 5503	2.000
9000-0301	FAN PAMOTOR 4600X	2.000
9010-6599	TRANSFORMER TECO 6599	1.000
9110-0101	TERMINAL STRIP 6PIN EHS3006	1.000
9160-0003	CAPACITOR CLAMP 2IN O.C.	4.000
9525-4480	MF5 R/P INTERFACE ASSY	1.000
9555-4478	CABLE ASSY FLAT 40 PCS	1.000
9555-4589	MF5 AC/DC HARNESS ASSY	1.000
9705-4306	MF5 REAR PANEL	1.000
9705-4395	COVER PLATE	2.000
9705-4479	CABLE ASSY MOUNTING PANEL	1.000
9705-4509	RIGHT SIDE BRACKET	1.000
9705-4510	LEFT SIDE BRACKET	1.000
9705-4544	MF5 REAR PANEL GPIB LABEL	1.000
9705-4598	SUPPORT BRACKET	1.000

MFS GPIB REAR PANEL PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9203-0000	SWITCH PB MMNTRY SPST CK8121Z	1.000
9203-0003A	BLK PBSW CAP C&KA7089-2	1.000
9207-0002	SWITCH DIP SPST 8 SECTIONS	1.000
9306-0030	CONN RCE RCR MALE STRT 40 PCS	1.000
98ART-54475	MFS GPIB REAR PANEL PCB	1.000
98SCH-54474	MFS GPIB REAR PANEL	1.000
9605-4475	MFS GPIB REAR PANEL PCB	1.000
9795-4588	CONNECTOR REWORKED	1.000

MF5 R/P INTERFACE ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8C0C-0043	SCREW PNHD MET NC.4-40X1/4	1.0CC
8000-1202	LCCKWASHER NC.4 INT TCCTH	2.0CC
8C00-1302	FLAT WASHER MET NC.4	1.CCC
8000-2304	SPACER MET HEX THD 4-40X1/2	2.CCC
8000-9002	METRIC STUD MNT STANDOFF SET	2.CCO
9545-4476	MF5 GPIB REAR PANEL PCB ASSY	1.CCC
9705-4470	GPIB INTERFACE REAR PANEL	1.CCC

MFS GPIB OPTION

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9525-4328RETRO	MFS REAR PANEL ASSY GPIBRETRO	1.000
9535-4347RETRO	MFS CHASSIS ASSY GPIB RETRO	1.000

MFS REAR PANEL ASSY GPIBRETRC

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0045	SCREW PNHD MET NO.4-40X3/8	8.000
8000-1001	NUT HEX MET NO.3-48	2.000
8000-1002	NUT HEX MET NO.4-40	8.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	8.000
9525-4480	MFS R/P INTERFACE ASSY	1.000
9555-4478	CABLE ASSY FLAT 40 POS	1.000
9705-4479	CABLE ASSY MOUNTING PANEL	1.000
9705-4544	MFS REAR PANEL GPIB LABEL	1.000

MF5 CHASSIS ASSY GPIB RETRC

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0045	SCREW PNHD MET NO.4-40X3/8	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
9525-4477	MF5 GPIB MOUNTING PANEL ASSY	1.000
9535-4603RETRC	CONN BRKT PWRD I/C GPIB RETRC	1.000
9705-4467	FRONT PANEL BRACKET	1.000

CONN BRKT PWR & I/O ASSY GPIB

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0045	SCREW PNHD MET NO.4-40X3/8	16.000
8000-0085	SCREW PNHD MET NO.6-32X3/8	4.000
8000-1002	NUT HEX MET NO.4-40	8.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	16.000
8000-1204	LOCKWASHER NO.6 INT TOOTH	4.000
8000-9017	PIN MALE MOLEX 02-09-2103	6.000
9300-0104	CONN RECEPT 24 PCS	4.000
9318-0005	CONN PLUG 6 POS 03-09-2062	1.000
9555-4479	CABLE ASSY FLAT 50 PCS	1.000
9705-4307	AIR DEFLECTOR BAFFLE	2.000
9705-4599	CONNECTOR BRACKET	1.000

MFS GPIB MOUNTING PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0043	SCREW PNHD MET NC.4-40X1/4	4.000
8000-0047	SCREW PNHD MET NC.4-40X1/2	2.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	6.000
8000-1302	FLAT WASHER MET NO.4	2.000
8000-2313	SPACER MET HEX THD 4-40X1 1/4	2.000
8000-2606	SPACER MET ML/FML 4-40 X 1	2.000
9545-4473	MFS GPIB MOTHER BD PCB ASSY	1.000
9545-4545	BUS INTERFACE PCB REWORK	1.000
9705-4468	GPIB MOUNTING PANEL	1.000

BUS INTERFACE PCB REWORK

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9540-0001	IEEE 488 BUS INTERFACE PCB	1.000

TABLE 7-2

MS-302

Clock Source

MS302 CLOCK SOURCE

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0043	SCREW PNHD MET NO.4-40X1/4	6.000
8000-0071	SCREW PNHD MET NO.5-40X1/4	6.000
8000-0072	SCREW PNHD MET NO.5-40X3/8	8.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	6.000
8000-1203	LOCKWASHER NO.5 INT TOOTH	6.000
8000-9020	MODULE THUMBSCREW B-63013	2.000
9303-0004	PIN RECEPTACLE SNAP-IN	6.000
9515-4496	MS302 FRONT PANEL ASSY	1.000
9525-4496	MS302 REAR PANEL ASSY	1.000
9535-4496	MS302 ECOST TRNSTR PANEL ASSY	1.000
9545-4514	MS302 CLOCK SOURCE PCB ASSY	1.000
9545-4517	MS302 XTAL OSC PCB ASSY	1.000
9555-4567	CABLE ASSY COAXIAL	3.000
9705-4410	MODULE SIDE COVER	1.000
9705-4528	BERTS 325 MODULE RAILS	1.000

MS302 FRONT PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0333-41C0E	RES VAR 1 KOHM 10P 1/2W	1.000
8C00-0043	SCREW PNHD MET NO.4-40X1/4	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
9303-0004	PIN RECEPTACLE SNAP-ON	8.000
9545-4495	MS302 FRONT PANEL PCB ASSY	1.000
9555-4562	CABLE ASSY COAXIAL	2.000
9705-4490	MS302 FRONT PANEL FINISHED	1.000
9725-4492	MS302 DISPLAY WINDOW	1.000
9735-6414	SPACER MET HEX 0.531 LG	4.000
9801-672AM	KNOB .92D X .64LG BLK 1/4 SHFT	1.000

MS302 REAR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-2120	RES COMP 12 OHM 5P 1/4W	1.000
0022-3150	RES COMP 150 OHM 5P 1/4W	1.000
0022-3300	RES COMP 300 OHM 5P 1/4W	2.000
1014-4610	CAP CER 0.1 MFD 20P 200V	1.000
1024-5110	CAP ELEC 1 MFD 35WVDC	2.000
1024-5147	CAP ELEC 4.7 MFD 20P 35WVDC	1.000
1024-5210	CAP ELEC 10 MFD 35WVDC	2.000
2101-4001	DIODE RECTIFIER 1N4001	2.000
4200-340K5	IC LINEAR REGULATOR LM340K5	1.000
4201-320K5	IC LINEAR REGULATOR LM320K5	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	6.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	1.000
8000-1506	LUG SOLDER ANGLE NO.4	5.000
8000-6000	BUSHING INSULATING TO-3	4.000
8000-6001	WASHER INSULATING TO-3	2.000
8000-6002	SOCKET TO-3 MOUNTING	2.000
9300-0103	CONN PLUG PANEL MNT 24 PCS	1.000
9705-4448	MODULE 4IN REAR PANEL MACHINED	1.000

MS302 BOOST TRNSTR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-1300	RES COMP 3 OHM 5P 1/4W	1.000
1014-4610	CAP CER 0.1 MFD 20P 200V	1.000
1024-5110	CAP ELEC 1 MFD 35WVDC	2.000
1024-5147	CAP ELEC 4.7 MFD 20P 35WVDC	1.000
3180-3055	TRNSTR NPN POWER 2N3055	1.000
4200-340K15	IC LINEAR REGULATOR LM340K15	1.000
4201-320K15	IC LINEAR REGULATOR LM320K15	1.000
8000-0047	SCREW PNHD MET NO.4-40X1/2	6.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	6.000
8000-1002	NUT HEX MET NO.4-40	6.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	2.000
8000-1506	LUG SOLDER ANGLE NO.4	4.000
8000-6000	BUSHING INSULATING TO-3	6.000
8000-6001	WASHER INSULATING TO-3	3.000
8000-6002	SOCKET TO-3 MOUNTING	3.000
9705-4174	BOOST TRNSTR PANEL	1.000

MS302 FRONT PANEL PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-3100	RES COMP 100 OHM 5P 1/4W	1.000
0022-3220	RES COMP 220 OHM 5P 1/4W	8.000
0022-3300	RES COMP 300 OHM 5P 1/4W	2.000
0022-4100	RES COMP 1 KOHM 5P 1/4W	2.000
0022-5100	RES COMP 10 KOHM 5P 1/4W	4.000
0022-8220	RES COMP 22 MOHM 5P 1/4W	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	2.000
1042-9256	CAP MICA 56 PF 5P 500V	1.000
1059-8260	CAP VAR 15-60 PF PC MNT 200V	1.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	2.000
2112-4148	DIODE GEN PURPOSE IN4148	1.000
2274-5374	DIODE LED YELLOW MV5374C	9.000
3224-4403	TRNSTR NPN AMPLIFIER 2N4403	2.000
4012-7445	IC TTL SN7445N PLSTC	1.000
4074-7216D	IC DISPLAY/DRIVER ICM7216D	1.000
4513-7433	IC DISPLAY ARRAY HP5082-7433	2.000
6000-6116	XTAL 10.000 MHZ	1.000
6900-0000	XTAL SOCKET HC-25/U	1.000
8000-0001	SCREW PNHD MET NO.2-56X1/4	1.000
8000-1000	NUT HEX MET NO.2-56	1.000
8000-1200	LOCKWASHER NO.2 INT TOOTH	1.000
8000-2903	SPACER NYLON 3/16OD X 7/16LG	9.000
9205-0011	SWITCH PB MAINTAINED LTD YEL	1.000
9205-0019	SWITCH PB MOMENTARY NO LED	3.000
9300-0138	SOCKET IC 28 PIN LOW PROFILE	1.000
9300-0148	SOCKET STRIP 12 PIN	2.000
9300-0149	CONN EDGE DUAL 15 POS PC MNT	1.000
9303-0003	CONN POST MALE	4.000
9605-4494	MS302 FRONT PANEL PCB	1.000

MS302 CLOCK SOURCE PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-1560	RES COMP 5.6 OHM 5P 1/8W	2.000
0012-2150	RES COMP 15 OHM 5P 1/8W	2.000
0012-2390	RES COMP 39 OHM 5P 1/8W	1.000
0012-2470	RES COMP 47 OHM 5P 1/8W	2.000
0012-2510	RES COMP 51 OHM 5P 1/8W	2.000
0012-2820	RES COMP 82 OHM 5P 1/8W	2.000
0012-3100	RES COMP 100 OHM 5P 1/8W	38.000
0012-3120	RES COMP 120 OHM 5P 1/8W	1.000
0012-3130	RES COMP 130 OHM 5P 1/8W	2.000
0012-3150	RES COMP 150 OHM 5P 1/8W	2.000
0012-3160	RES COMP 160 OHM 5P 1/8W	4.000
0012-3270	RES COMP 270 OHM 5P 1/8W	4.000
0012-3470	RES COMP 470 OHM 5P 1/8W	12.000
0012-3510	RES COMP 510 OHM 5P 1/8W	1.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	6.000
0012-4200	RES COMP 2 KOHM 5P 1/8W	4.000
0012-4510	RES COMP 5.1 KOHM 5P 1/8W	1.000
0012-4750	RES COMP 7.5 KOHM 5P 1/8W	1.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	4.000
0012-5150	RES COMP 15 KOHM 5P 1/8W	4.000
0012-5200	RES COMP 20 KOHM 5P 1/8W	3.000
0022-2750	RES COMP 75 OHM 5P 1/4W	1.000
0022-3120	RES COMP 120 OHM 5P 1/4W	1.000
0333-2100	RES VAR 10 OHM 10P 1/2W	2.000
0333-3500J	RES VAR 500 OHM 10P 1/2W	2.000
0333-4100	RES VAR 1 KOHM 10P 1/2W	3.000
0333-4100T	RES VAR 1 KOHM 10P 1/2W	5.000
0333-4500	RES VAR 5 KOHM 10P 1/2W	1.000
0333-5100	RES VAR 10 KOHM 10P 3/4W	1.000
0333-5100C	RES VAR 10 KOHM 10P 1/2W	1.000
1014-4610	CAP CER 0.1 MFD 20P 200V	1.000
1024-5110	CAP ELEC 1 MFD 35WVDC	3.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	2.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	1.000
1084-4710	CAP CHIP .01 MFD 50WVDC	105.000
2112-4148	DIODE GEN PURPOSE IN4148	1.000
2143-1403	DIODE VARACTOR MV1403	2.000
4012-10124	IC ECL MC10124P PLSTC	2.000
4012-10125	IC ECL MC10125P PLSTC	1.000
4012-10138	IC ECL MC10138P PLSTC	4.000
4012-1658L	IC ECL MC1658L CER	1.000
4012-4000	IC CMOS MC14000BCP PLSTC	1.000
4012-4490	IC CMOS MC14490BCP PLSTC	1.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS151	IC TTL SN74LS151N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	1.000
4012-74LS193	IC TTL SN74LS193N PLSTC	2.000

MS302 CLOCK SOURCE PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
4012-7404	IC TTL SN7404N PLSTC	1.000
4012-7417	IC TTL SN7417N PLSTC	1.000
4012-8620	IC ECL SP8620B	1.000
4012-8630B	IC ECL SP8630B CER DIP	1.000
4055-0102	IC ECL F100102FC	2.000
4055-0114	IC ECL F100114FC	1.000
4055-0131	IC ECL F100131FC	1.000
4055-0164	IC ECL F100164FC	1.000
4055-0171	IC ECL F100171FC	1.000
4110-1458	IC OPAMP MC1458CP1	1.000
4200-340T5	IC LINEAR REGULATOR LM340T5	1.000
4201-337T	IC LINEAR REGULATOR LM337T	1.000
5924-0T41	XFMR DC ISOL T4-1	3.000
5925-08T6	8T6 RF XMFR 50/100 OHM CT	1.000
6100-0002	XTAL VCO 165-330MHZ VL371-5789	1.000
7000-0001	RELAY 8 PIN DIP D2A05	2.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	2.000
8000-1002	NUT HEX MET NO.4-40	2.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	2.000
8000-1421	WASHER MICA NO.4	2.000
9100-0118	HEAT SINK PCB MNT TO-220	2.000
9201-0002	SWITCH SLIDE DPDT MSS225D	2.000
9301-0060A	CONN COAXIAL PCB MNT	5.000
9303-0003	CONN POST MALE	6.000
9306-0004	SOCKET PIN LOW PROFILE	24.000
9306-0034	CONN PCB HDR MALE STRT 20 POS	1.000
9314-0011	STIK POST 0.10 CTRS	2.000
9314-0012	JUMPER FOR STIK POST 0.10 CTRS	1.000
9565-9083	MASSON MCKT ASSY	2.000
9605-4513	MS302 CLOCK SOURCE PCB	1.000

MS302 XTAL OSC PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-2390	RES COMP 39 OHM 5P 1/8W	3.000
0012-3150	RES COMP 150 OHM 5P 1/8W	6.000
0022-2100	RES COMP 10 OHM 5P 1/4W	3.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	3.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	2.000
7000-0001	RELAY 8 PIN DIP D2AC5	3.000
8000-1004	NUT HEX MET NO.6-32	12.000
8000-1204	LOCKWASHER NO.6 INT TOOTH	12.000
8000-1304	FLAT WASHER MET NO.6	12.000
9300-0150	PRINTED WIRING CONTACTS	15.000
9303-0003	CONN POST MALE	6.000
9605-4516	MS302 XTAL OSC PCB	1.000

MS302 GPIB OPTION KIT

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0043	SCREW PNHD MET NC.4-40X1/4	4.000
8000-0047	SCREW PNHD MET NC.4-40X1/2	2.000
8000-0614	SCREW FLTHD MET NC.4-40X5/16	12.000
8000-1002	NUT HEX MET NC.4-40	2.000
8000-1202	LOCKWASHER NC.4 INT TOOTH	6.000
8000-1302	FLAT WASHER MET NC.4	2.000
9545-4541	MS302 GPIB ADAPTER PCB ASSY	1.000
9555-4440	CABLE ASSY FLAT 50 POS	1.000
9555-4552	CABLE ASSY FLAT 20 POS	1.000
9705-4434	PC CARD HOLDER BRACKET	2.000
9705-4486	PC HOLDER BRACKET	4.000

MS302 GPIB ADAPTER PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-4300	RES COMP 3 KOHM 5P 1/8W	7.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	13.000
1054-1233	CAP MIN-TANT 33 MFD 10WVDC	1.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS04	IC TTL SN74LS04N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	2.000
4012-74LS174	IC TTL SN74LS174N PLSTC	2.000
4012-7485	IC TTL SN7485N PLSTC	1.000
9303-0003	CONN POST MALE	2.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
9306-0044	CONN PCB HDR MALE RTANGL 20 PCS	1.000
9314-0011	STIK POST 0.10 CTRS	3.000
9314-0012	JUMPER FOR STIK POST 0.10 CTRS	3.000
9605-4482	GPIB ADAPTER PCB	1.000

Table 7-3

MN-302

BERT Transmitter

MN302 PSEUDORANDOM GENERATOR

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	6.000
8000-0071	SCREW PNHD MET NO.5-40X1/4	6.000
8000-0072	SCREW PNHD MET NO.5-40X3/8	8.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	6.000
8000-1203	LOCKWASHER NO.5 INT TOOTH	6.000
8000-9020	MODULE THUMBSCREW B-63013	2.000
9303-0092A	HEX NUT FOR 9303-0092	4.000
9515-4411	MN302 FRONT PANEL ASSY	1.000
9525-4411	MN302 REAR PANEL ASSY	1.000
9535-4411	MN302 BOOST TRNSTR PANEL ASSY	1.000
9545-4356	MN302 CODE GENERATOR PCB ASSY	1.000
9545-4454	MN302 OPTOL INTERFACE PCB ASSY	1.000
9555-4439	CABLE ASSY FLAT 16 PCS	1.000
9705-4410	MODULE SIDE COVER	1.000
9705-4528	BERTS 325 MODULE RAILS	1.000

MN302 FRONT PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
9303-0004	PIN RECEPTACLE SNAP-ON	6.000
9545-4353	MN302 F/P DISPLAY BD ASSY	1.000
9555-4563	CABLE ASSY COAXIAL	3.000
9555-4564	CABLE ASSY COAXIAL	1.000
9705-4405	MN302 FRONT PANEL FINISHED	1.000
9735-6414	SPACER MET HEX 0.531 LG	4.000

MN302 REAR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-2120	RES COMP 12 OHM 5P 1/4W	1.000
0022-3150	RES COMP 150 OHM 5P 1/4W	1.000
0022-3300	RES COMP 300 OHM 5P 1/4W	2.000
1014-4610	CAP CER 0.1 MFD 20P 200V	1.000
1024-5110	CAP ELEC 1 MFD 35WVDC	2.000
1024-5147	CAP ELEC 4.7 MFD 20P 35WVDC	1.000
1024-5210	CAP ELEC 10 MFD 35WVDC	2.000
2101-4001	DIODE RECTIFIER 1N4001	2.000
4200-340K5	IC LINEAR REGULATOR LM340K5	1.000
4201-320K5	IC LINEAR REGULATOR LM320K5	1.000
8000-0047	SCREW PNHD MET NO.4-40X1/2	6.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	1.000
8000-1506	LUG SOLDER ANGLE NO.4	5.000
8000-6000	BUSHING INSULATING TO-3	4.000
8000-6001	WASHER INSULATING TO-3	2.000
8000-6002	SOCKET TO-3 MOUNTING	2.000
9300-0103	CONN PLUG PANEL MNT 24 POS	1.000
9705-4448	MODULE 4IN REAR PANEL MACHINED	1.000

MN302 BCCST TRNSTR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTICN	QUANTITY PER
0022-1300	RES COMP 3 CHM 5P 1/4W	1.000
3180-3055	TRNSTR NPN PCWER 2N3055	1.000
8000-0047	SCREW PNHD MET NC.4-40X1/2	2.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	2.000
8000-1002	NUT HEX MET NO.4-40	2.000
8000-1202	LCCKWASHER NO.4 INT TCOTH	2.000
8000-6000	BUSHING INSULATING TC-3	2.000
8000-6001	WASHER INSULATING TC-3	1.000
8000-6002	SCCKET TC-3 MOUNTING	1.000
9705-3283	BCOST TRANSISTOR PANEL	1.000

MN302 F/P DISPLAY BD ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-1560	RES COMP 5.6 OHM 5P 1/8W	1.000
0012-2470	RES COMP 47 OHM 5P 1/8W	1.000
0012-2510	RES COMP 51 OHM 5P 1/8W	2.000
0012-3100	RES COMP 100 OHM 5P 1/8W	1.000
0012-3150	RES COMP 150 OHM 5P 1/8W	6.000
0012-3160	RES COMP 160 OHM 5P 1/8W	1.000
0012-3200	RES COMP 200 OHM 5P 1/8W	5.000
0012-3270	RES COMP 270 OHM 5P 1/8W	1.000
0012-3300	RES COMP 300 OHM 5P 1/8W	3.000
0012-3390	RES COMP 390 OHM 5P 1/8W	1.000
0012-3470	RES COMP 470 OHM 5P 1/8W	3.000
0012-3910	RES COMP 910 OHM 5P 1/8W	1.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	3.000
0012-4150	RES COMP 1.5 KOHM 5P 1/8W	3.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	1.000
0022-2510	RES COMP 51 OHM 5P 1/4W	2.000
0333-2100	RES VAR 10 OHM 10P 1/2W	1.000
0333-3500J	RES VAR 500 OHM 10P 1/2W	1.000
0333-4100	RES VAR 1 KOHM 10P 1/2W	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	9.000
1064-3747	CAP MIN-TANT 4.7 MFD 20WVDC	2.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	1.000
1084-4710	CAP CHIP .01 MFD 50WVDC	5.000
2101-4001	DIODE RECTIFIER IN4001	1.000
2112-4148	DIODE GEN PURPOSE IN4148	1.000
2274-5374	DIODE LED YELLOW MV5374C	7.000
2274-5774	DIODE LED RED MV5774C	2.000
3224-4403	TRNSTR NPN AMPLIFIER 2N4403	6.000
4012-10198	IC ECL MC10198P PLSTC	1.000
8000-2903	SPACER NYLON 3/16OD X 7/16LG	9.000
9201-0003	SWITCH SLIDE DP4T SS24	1.000
9201-0007	SWITCH SLIDE DPDT MSSA2350	1.000
9205-0011	SWITCH PB MAINTAINED LTD YEL	3.000
9205-0012	SWITCH PB MOMENTARY LTD YEL	1.000
9303-0003	CONN POST MALE	6.000
9303-0092	BNC RECEPTACLE PCB MNT	4.000
9306-0004	SOCKET PIN LOW PROFILE	12.000
9313-0001	CONN EDGE DUAL 22 POS PC MNT	1.000
9565-9083	MASSON MCKT ASSY	1.000
96ART-54352	MN302 FRONT PANEL DISPLAY PCB	1.000
96SCH-54351	MN302 FRONT PANEL DISPLAY	1.000
9605-4352	MN302 FRONT PANEL DISPLAY PCB	1.000

MN302 CODE GENERATOR PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-1560	RES COMP 5.6 OHM 5P 1/8W	3.000
0012-2150	RES COMP 15 OHM 5P 1/8W	3.000
0012-2510	RES COMP 51 OHM 5P 1/8W	3.000
0012-2820	RES COMP 82 OHM 5P 1/8W	4.000
0012-3100	RES COMP 100 OHM 5P 1/8W	25.000
0012-3130	RES COMP 130 OHM 5P 1/8W	4.000
0012-3160	RES COMP 160 OHM 5P 1/8W	2.000
0012-3270	RES COMP 270 OHM 5P 1/8W	2.000
0012-3470	RES COMP 470 OHM 5P 1/8W	60.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	5.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	2.000
0012-6100	RES COMP 100 KOHM 5P 1/8W	1.000
0022-2620	RES COMP 62 OHM 5P 1/4W	1.000
0022-3120	RES COMP 120 OHM 5P 1/4W	1.000
0333-2100	RES VAR 10 OHM 10P 1/2W	3.000
0333-3500J	RES VAR 500 OHM 10P 1/2W	3.000
0822-3100	RES SIP 8PIN 100 OHM 2P 0.3W	1.000
0822-3470	RES SIP 8PIN 470 OHM 2P 0.3W	7.000
1013-8510	CAP CER .01 MFD 20P 200V	41.000
1014-4610	CAP CER 0.1 MFD 20P 200V	4.000
1024-5110	CAP ELEC 1 MFD 35WVDC	3.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	4.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	5.000
1084-4710	CAP CHIP .01 MFD 50WVDC	29.000
2112-4148	DIODE GEN PURPOSE IN4148	7.000
4012-10102	IC ECL MC10102P PLSTC	2.000
4012-10105	IC ECL MC10105P PLSTC	1.000
4012-10124	IC ECL MC10124P PLSTC	1.000
4012-10125	IC ECL MC10125P PLSTC	1.000
4012-10138	IC ECL MC10138P PLSTC	1.000
4012-10141	IC ECL MC10141P PLSTC	5.000
4012-10172	IC ECL MC10172P PLSTC	1.000
4012-10178	IC ECL MC10178P PLSTC	2.000
4012-10211	IC ECL MC10211P PLSTC	2.000
4012-10231	IC ECL MC10231P PLSTC	6.000
4012-11C06	IC ECL F11C06DC CER	2.000
4012-1662L	IC ECL MC1662L CER	1.000
4012-1672L	IC ECL MC1672L CER	1.000
4012-1678L	IC ECL MC1678L CER	1.000
4012-1688F	IC ECL MC1688F CER	4.000
4012-74123	IC TTL SN74123N PLSTC	1.000
4055-0102	IC ECL F100102FC	1.000
4055-0107	IC ECL F100107FC	1.000
4055-0141	IC ECL F100141FC	1.000
4200-340T5	IC LINEAR REGULATOR LM340T5	1.000
4201-337T	IC LINEAR REGULATOR LM337T	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	2.000
8000-1002	NUT HEX MET NO.4-40	2.000

MN302 CODE GENERATOR PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-1202	LOCKWASHER NO.4 INT TOOTH	2.000
9201-0002	SWITCH SLIDE DPDT MSS225D	3.000
9301-0060A	CONN COAXIAL PCB MNT	4.000
9303-0003	CONN POST MALE	3.000
9303-0080	CONTACT PCB COAXIAL TERMNTR	2.000
9306-0004	SOCKET PIN LOW PROFILE	36.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	1.000
9565-9083	MASSOM MCKT ASSY	3.000
96ART-54355	MN302 CODE GEN PCB	1.000
96SCH-54354	MN302 CODE GEN	1.000
9605-4355	MN302 CODE GENERATOR PCB	1.000
9705-4416	HEAT SINK	1.000

MN302 OPTCL INTERFACE PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-4200	RES COMP 2 KOHM 5P 1/8W	1.000
0022-2430	RES COMP 43 OHM 5P 1/4W	3.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	5.000
1014-8410E	CAP CER 1000 PF 20P 100V 0.1SP	3.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	2.000
2274-0500	DIODE INFRARED FPE-500	3.000
4012-10125	IC ECL MC10125P PLSTC	1.000
4012-75472	IC LINEAR SN75472AN PLSTC	2.000
8000-0047	SCREW PNHD MET NC.4-40X1/2	2.000
8000-1302	FLAT WASHER MET NC.4	2.000
9303-0003	CONN POST MALE	3.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	2.000
96ART-54453	MN302 OPTICAL INTERFACE PCB	1.000
96SCH-54452	MN302 OPTICAL INTERFACE	1.000
9605-4453	MN302 OPTICAL INTERFACE PCB	1.000
9725-4459	PHOTOCELL MOUNTING BLOCK	1.000

MN302 GPIB OPTION KIT

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	4.000
8000-0047	SCREW PNHD MET NO.4-40X1/2	2.000
8000-0614	SCREW FLTHD MET NO.4-40X5/16	12.000
8000-1002	NUT HEX MET NO.4-40	2.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	18.000
8000-1302	FLAT WASHER MET NO.4	2.000
9303-0004	PIN RECEPTACLE SNAP-ON	3.000
9545-4539	MN302 GPIB ADAPTER PCB ASSY	1.000
9555-4440	CABLE ASSY FLAT 50 POS	1.000
9555-4553	CABLE ASSY FLAT 16 POS	1.000
9705-4434	PC CARD HOLDER BRACKET	2.000
9705-4486	PC HOLDER BRACKET	4.000

MN302 GPIB ADAPTER PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-3470	RES COMP 470 OHM 5P 1/8W	7.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	2.000
0012-4300	RES COMP 3 KOHM 5P 1/8W	8.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	16.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	2.000
4012-10124	IC ECL MC10124P PLSTC	2.000
4012-10125	IC ECL MC10125P PLSTC	2.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS04	IC TTL SN74LS04N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	2.000
4012-74LS174	IC TTL SN74LS174N PLSTC	2.000
4012-7485	IC TTL SN7485N PLSTC	1.000
9303-0003	CONN POST MALE	3.000
9306-0012	CONN RCE HDR 16 PIN 0.062 PCB	1.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
9314-0011	STIK POST C.10 CTRS	3.000
9314-0012	JUMPER FOR STIK POST C.10 CTRS	3.000
96ART-54482	GPIB ADAPTER PCB	1.000
96SCH-54481	GPIB ADAPTER	1.000
9605-4482	GPIB ADAPTER PCB	1.000

TABLE 7-4

MB-302

BERT Receiver

ME302 EERT RECEIVER

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	8.000
8000-0071	SCREW PNHD MET NO.5-40X1/4	8.000
8000-0072	SCREW PNHD MET NO.5-40X3/8	8.000
8000-0614	SCREW FLTHD MET NO.4-40X5/16	12.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	8.000
8000-1203	LOCKWASHER NO.5 INT TOOTH	8.000
8000-9020	MODULE THUMBSCREW B-63013	2.000
9303-0004	PIN RECEPTACLE SNAP-ON	8.000
9303-0092A	HEX NUT FOR 9303-0092	6.000
9515-4424	ME302 FRONT PANEL ASSY	1.000
9525-4424	MB302 REAR PANEL ASSY	1.000
9545-4362	MB302 COUNTER PCB ASSY	1.000
9545-4364	MB302 CODE RESYNC PCB ASSY	1.000
9545-4431	MB302 BCD INTERFACE PCB ASSY	1.000
9555-4439	CABLE ASSY FLAT 16 POS	2.000
9705-4410	MODULE SIDE COVER	2.000
9705-4433	PCB HOLDER BRACKET	4.000
9705-4434	PC CARD HOLDER BRACKET	2.000
9705-4528	BERTS 325 MODULE RAILS	1.000

ME302 FRONT PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
8000-0044	SCREW PNHD MET NO.4-40X5/16	4.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	4.000
9545-4359	ME302 F/P DISPLAY PC ASSY	1.000
9555-4559	CABLE ASSY COAXIAL	3.000
9705-4420	ME302 FRONT PANEL FINISHED	1.000
9725-4417	ME302 DISPLAY WINDOW	1.000
9735-6414	SPACER MET HEX 0.531 LG	4.000

ME302 REAR PANEL ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-1300	RES COMP 3 OHM 5P 1/4W	1.000
0022-2120	RES COMP 12 OHM 5P 1/4W	1.000
0022-3150	RES COMP 150 OHM 5P 1/4W	1.000
0022-3300	RES COMP 300 OHM 5P 1/4W	2.000
1014-4610	CAP CER 0.1 MFD 20P 200V	2.000
1024-5110	CAP ELEC 1 MFD 35WVDC	3.000
1024-5147	CAP ELEC 4.7 MFD 20P 35WVDC	1.000
1024-5210	CAP ELEC 10 MFD 35WVDC	2.000
2101-4001	DIODE RECTIFIER 1N4001	2.000
3180-3055	TRNSTR NPN POWER 2N3055	1.000
4200-340K5	IC LINEAR REGULATOR LM340K5	2.000
4201-320K5	IC LINEAR REGULATOR LM320K5	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	2.000
8000-0047	SCREW PNHD MET NO.4-40X1/2	10.000
8000-0808	SCREW SLF-TAP 6 X 1/2 TYPE B	8.000
8000-1002	NUT HEX MET NO.4-40	12.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	5.000
8000-1302	FLAT WASHER MET NO.4	4.000
8000-1506	LUG SOLDER ANGLE NO.4	7.000
8000-6000	BUSHING INSULATING TO-3	8.000
8000-6001	WASHER INSULATING TO-3	4.000
8000-6002	SOCKET TO-3 MOUNTING	4.000
9300-0103	CONN PLUG PANEL MNT 24 PCS	1.000
9555-4440	CABLE ASSY FLAT 50 PCS	1.000
9705-4426	ME302 REAR PANEL MACHINED	1.000

ME302 F/P DISPLAY BD ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-1560	RES COMP 5.6 OHM 5P 1/8W	2.000
0012-2330	RES COMP 33 OHM 5P 1/8W	6.000
0012-2470	RES COMP 47 OHM 5P 1/8W	2.000
0012-2510	RES COMP 51 OHM 5P 1/8W	2.000
0012-3120	RES COMP 120 OHM 5P 1/8W	7.000
0012-3160	RES COMP 160 OHM 5P 1/8W	1.000
0012-3220	RES COMP 220 OHM 5P 1/8W	12.000
0012-3270	RES COMP 270 OHM 5P 1/8W	3.000
0012-3390	RES COMP 390 OHM 5P 1/8W	2.000
0012-3470	RES COMP 470 OHM 5P 1/8W	6.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	4.000
0012-4470	RES COMP 4.7 KOHM 5P 1/8W	2.000
0012-4510	RES COMP 5.1 KOHM 5P 1/8W	1.000
0012-6200	RES COMP 200 KOHM 5P 1/8W	1.000
0022-2510	RES COMP 51 OHM 5P 1/4W	6.000
0022-3750	RES COMP 750 OHM 5P 1/4W	2.000
0333-2100	RES VAR 10 OHM 10P 1/2W	2.000
0333-3500J	RES VAR 500 OHM 10P 1/2W	2.000
0333-4100T	RES VAR 1 KOHM 10P 1/2W	2.000
1013-8510	CAP CER .01 MFD 20P 200V	7.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	17.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	4.000
1064-4210	CAP MIN-TANT 10 MFD 25WVDC	4.000
1084-4710	CAP CHIP .01 MFD 50WVDC	4.000
2112-4148	DIODE GEN PURPOSE IN4148	2.000
2274-5274	DIODE LED GREEN MV5274C	2.000
2274-5374	DIODE LED YELLOW MV5374C	9.000
2274-5774	DIODE LED RED MV5774C	5.000
3224-4401	TRNSTR NPN AMPLIFIER 2N4401	6.000
3224-4403	TRNSTR NPN AMPLIFIER 2N4403	2.000
4012-4490	IC CMOS MC14490BCP PLSTC	1.000
4012-4520	IC CMOS MC14520BCP PLSTC	1.000
4012-74C912	IC CMOS MM74C912	1.000
4012-74LS08	IC TTL SN74LS08N PLSTC	2.000
4012-74S139	IC TTL SN74S139N PLSTC	2.000
4012-7408	IC TTL SN7408N PLSTC	1.000
4513-0308	IC DISPLAY TIL308	1.000
4513-7653	IC DISPLAY HP 5082-7653	6.000
4513-7736	IC DISPLAY HP 5082-7736	1.000
8000-2403	SPACER INSL CLRNC 4 X 7/16	16.000
9201-0003	SWITCH SLIDE DP4T SS24	1.000
9201-0007	SWITCH SLIDE DPDT MSSA2350	3.000
9205-0011	SWITCH PB MAINTAINED LTD YEL	1.000
9205-0012	SWITCH PB MOMENTARY LTD YEL	7.000
9300-0030	SOCKET IC 16 PIN LOW PROFILE	1.000
9300-0048	SOCKET IC 14 PIN LOW PROFILE	7.000
9303-0081	CONN EDGE DUAL 22 POS PC MNT	1.000
9303-0082	CONN EDGE DUAL 35 POS PC MNT	1.000

MB302 F/P DISPLAY BD ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9303-0092	BNC RECEPTACLE PCB MNT	6.000
9306-0004	SOCKET PIN LOW PROFILE	24.000
9306-0034	CONN PCB HDR MALE STRT 20 POS	1.000
9306-0035	CONN SOCKET FEMALE 20 POS	1.000
9565-9083	MASSOM MCKT ASSY	2.000
96ART-54358	MB302 FRONT PANEL DISPLAY PCB	1.000
96SCH-54357	MB302 FRONT PANEL DISPLAY	1.000
9605-4358	MB302 FRONT PANEL DISPLAY PCB	1.000

MB302 COUNTER PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-3180	RES COMP 180 OHM 5P 1/8W	2.000
0012-3390	RES COMP 390 OHM 5P 1/8W	2.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	10.000
0012-4200	RES COMP 2 KOHM 5P 1/8W	16.000
0012-4470	RES COMP 4.7 KOHM 5P 1/8W	1.000
0012-4510	RES COMP 5.1 KOHM 5P 1/8W	1.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	1.000
0012-5510	RES COMP 51 KOHM 5P 1/8W	1.000
1013-8310	CAP CER 100 PF 20P 200V	2.000
1013-8322	CAP CER 220 PF 20P 200V	1.000
1013-8347	CAP CER 470 PF 20P 200V	1.000
1013-8510	CAP CER .01 MFD 20P 200V	30.000
1064-0847	CAP MIN-TANT 47 MFD 6WVDC	2.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	2.000
2112-4148	DIODE GEN PURPOSE IN4148	3.000
4012-4072	IC CMOS MC14072BCP PLSTC	1.000
4012-74LS00	IC TTL SN74LS00N PLSTC	2.000
4012-74LS04	IC TTL SN74LS04N PLSTC	2.000
4012-74LS08	IC TTL SN74LS08N PLSTC	5.000
4012-74LS123	IC TTL SN74LS123N PLSTC	1.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS151	IC TTL SN74LS151N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	3.000
4012-74LS161	IC TTL SN74LS161N PLSTC	2.000
4012-74LS192	IC TTL SN74LS192N PLSTC	1.000
4012-74LS257	IC TTL SN74LS257N PLSTC	6.000
4012-74LS32	IC TTL SN74LS32N PLSTC	3.000
4012-74LS490	IC TTL SN74LS490N PLSTC	9.000
4012-74LS74	IC TTL SN74LS74N PLSTC	5.000
4012-74276	IC TTL SN74276N PLSTC	2.000
4012-74390	IC TTL SN74390N PLSTC	1.000
4160-0555	IC LINEAR NE555N	1.000
9080-1001	OSC 1 MHZ 14 PIN DIP	1.000
9300-0048	SOCKET IC 14 PIN LOW PROFILE	1.000
9303-0003	CONN POST MALE	2.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	2.000
9314-0011	STIK POST 0.10 CTRS	6.000
9314-0012	JUMPER FOR STIK POST 0.10 CTRS	2.000
96ART-54361	MB302 COUNTER PCB	1.000
96SCH-54360	MB302 COUNTER	1.000
9605-4361	MB302 COUNTER PCB	1.000

MB302 CODE RESYNC PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-2510	RES COMP 51 OHM 5P 1/8W	11.000
0012-2750	RES COMP 75 OHM 5P 1/8W	3.000
0012-3100	RES COMP 100 OHM 5P 1/8W	74.000
0012-3470	RES COMP 470 OHM 5P 1/8W	14.000
0012-4100	RES COMP 1 KOHM 5P 1/8W	11.000
0012-5100	RES COMP 10 KOHM 5P 1/8W	1.000
0022-2750	RES COMP 75 OHM 5P 1/4W	1.000
0022-3120	RES COMP 120 OHM 5P 1/4W	1.000
0333-4100T	RES VAR 1 KOHM 10P 1/2W	2.000
0822-3100	RES SIP 8PIN 100 OHM 2P 0.3W	8.000
0822-3470	RES SIP 8PIN 470 OHM 2P 0.3W	2.000
1013-8510	CAP CER .01 MFD 20P 200V	67.000
1014-8410	CAP CER 1000 PF 20P 200V	3.000
1024-5110	CAP ELEC 1 MFD 35WVDC	2.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	6.000
1064-3747	CAP MIN-TANT 4.7 MFD 20WVDC	1.000
1084-4710	CAP CHIP .01 MFD 50WVDC	8.000
2112-4148	DIODE GEN PURPOSE IN4148	1.000
4012-10H116	IC ECL MC10H116P PLSTC DIP	1.000
4012-10016	IC ECL F10016DC CER	1.000
4012-10102	IC ECL MC10102P PLSTC	4.000
4012-10105	IC ECL MC10105P PLSTC	1.000
4012-10124	IC ECL MC10124P PLSTC	3.000
4012-10125	IC ECL MC10125P PLSTC	3.000
4012-10131	IC ECL MC10131P PLSTC	1.000
4012-10141	IC ECL MC10141P PLSTC	5.000
4012-10178	IC ECL MC10178P PLSTC	1.000
4012-10198	IC ECL MC10198P PLSTC	1.000
4012-10211	IC ECL MC10211P PLSTC	2.000
4012-10212	IC ECL MC10212P PLSTC	1.000
4012-10231	IC ECL MC10231P PLSTC	6.000
4012-11C70	IC ECL F11C70DC CER	1.000
4012-1662L	IC ECL MC1662L CER	4.000
4012-1672L	IC ECL MC1672L CER	1.000
4012-1678L	IC ECL MC1678L CER	2.000
4012-1688F	IC ECL MC1688F CER	4.000
4012-1692L	IC ECL MC1692L CER	1.000
4055-0102	IC ECL F100102FC	1.000
4055-0131	IC ECL F100131FC	1.000
4201-337T	IC LINEAR REGULATOR LM337T	1.000
8000-0045	SCREW PNHD MET NO.4-40X3/8	1.000
8000-1002	NUT HEX MET NO.4-40	1.000
8000-1202	LOCKWASHER NO.4 INT TOOTH	1.000
9100-0116	HEAT SINK FOR TAB MNT TRNSTR	1.000
9301-0060A	CONN COAXIAL PCB MNT	3.000
9303-0003	CONN POST MALE	4.000
96ART-54365	MB302 CODE RESYNC PCB	1.000
96SCH-54364	MB302 CODE RESYNC	1.000
9605-4365	MB302 CODE RESYNC PCB	1.000

MB302 BCD INTERFACE PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0022-3100	RES COMP 100 OHM 5P 1/4W	1.000
0022-3180	RES COMP 180 OHM 5P 1/4W	4.000
0022-3390	RES COMP 390 OHM 5P 1/4W	4.000
0022-4200	RES COMP 2 KOHM 5P 1/4W	18.000
0022-5100	RES COMP 10 KOHM 5P 1/4W	3.000
0333-6100B	RES VAR 100 KOHM 10P 1.25W	2.000
1013-8233	CAP CER 33 PF 20P 200V	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	6.000
1014-8410E	CAP CER 1000 PF 20P 100V 0.1SP	1.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	1.000
1064-3747	CAP MIN-TANT 4.7 MFD 20WVDC	2.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS02	IC TTL SN74LS02N PLSTC	3.000
4012-74LS04	IC TTL SN74LS04N PLSTC	2.000
4012-74LS11	IC TTL SN74LS11N PLSTC	1.000
4012-74LS123	IC TTL SN74LS123N PLSTC	2.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	3.000
4012-74LS175	IC TTL SN74LS175N PLSTC	6.000
4012-74LS74	IC TTL SN74LS74N PLSTC	1.000
4012-74LS76A	IC TTL SN74LS76AN PLSTC	1.000
4012-7407	IC TTL SN7407N PLSTC	1.000
9303-0003	CONN POST MALE	2.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	2.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
96ART-54430	MB302 BCD INTERFACE PCB	1.000
96SCH-54429	MB302 BCD INTERFACE	1.000
9605-4430	MB302 BCD INTERFACE PCB	1.000

MB302 GPIB OPTION KIT

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
9545-4543	MB302 GPIB ADAPTER PCB ASSY	1.000
9555-4552	CABLE ASSY FLAT 20 PCS	1.000

MB302 GPIB ADAPTER PCB ASSY

COMPONENT ITEM NO.	DESCRIPTION	QUANTITY PER
0012-3100	RES COMP 100 OHM 5P 1/8W	1.000
0012-3180	RES COMP 180 OHM 5P 1/8W	4.000
0012-3390	RES COMP 390 OHM 5P 1/8W	4.000
0012-4300	RES COMP 3 KOHM 5P 1/8W	25.000
0012-4510	RES COMP 5.1 KOHM 5P 1/8W	2.000
1013-8315	CAP CER 150 PF 10P 200V	1.000
1013-8510E	CAP CER .01 MFD 20P 100V 0.1SP	19.000
1014-8210	CAP CER 10 PF 20P 200V	1.000
1014-8410	CAP CER 1000 PF 20P 200V	1.000
1064-1233	CAP MIN-TANT 33 MFD 10WVDC	1.000
4012-74LS00	IC TTL SN74LS00N PLSTC	1.000
4012-74LS02	IC TTL SN74LS02N PLSTC	1.000
4012-74LS04	IC TTL SN74LS04N PLSTC	2.000
4012-74LS11	IC TTL SN74LS11N PLSTC	1.000
4012-74LS123	IC TTL SN74LS123N PLSTC	1.000
4012-74LS138	IC TTL SN74LS138N PLSTC	1.000
4012-74LS157	IC TTL SN74LS157N PLSTC	7.000
4012-74LS174	IC TTL SN74LS174N PLSTC	2.000
4012-74LS175	IC TTL SN74LS175N PLSTC	7.000
4012-74LS74	IC TTL SN74LS74N PLSTC	1.000
4012-74LS76A	IC TTL SN74LS76AN PLSTC	1.000
4012-7407	IC TTL SN7407N PLSTC	1.000
4012-7485	IC TTL SN7485N PLSTC	2.000
9303-0003	CONN POST MALE	2.000
9306-0012	CONN PCB HDR 16 PIN 0.062 PCB	2.000
9306-0039	CONN PCB HDR MALE 50 POS	1.000
9306-0044	CONN PCB HDR MALE RTAGL 20 POS	1.000
9314-0011	STIK POST 0.10 CTRS	3.000
9314-0012	JUMPER FOR STIK POST 0.10 CTRS	3.000
96ART-54482	GPIB ADAPTER PCB	1.000
96SCH-54481	GPIB ADAPTER	1.000
9605-4482	GPIB ADAPTER PCB	1.000

8. DIAGRAMS

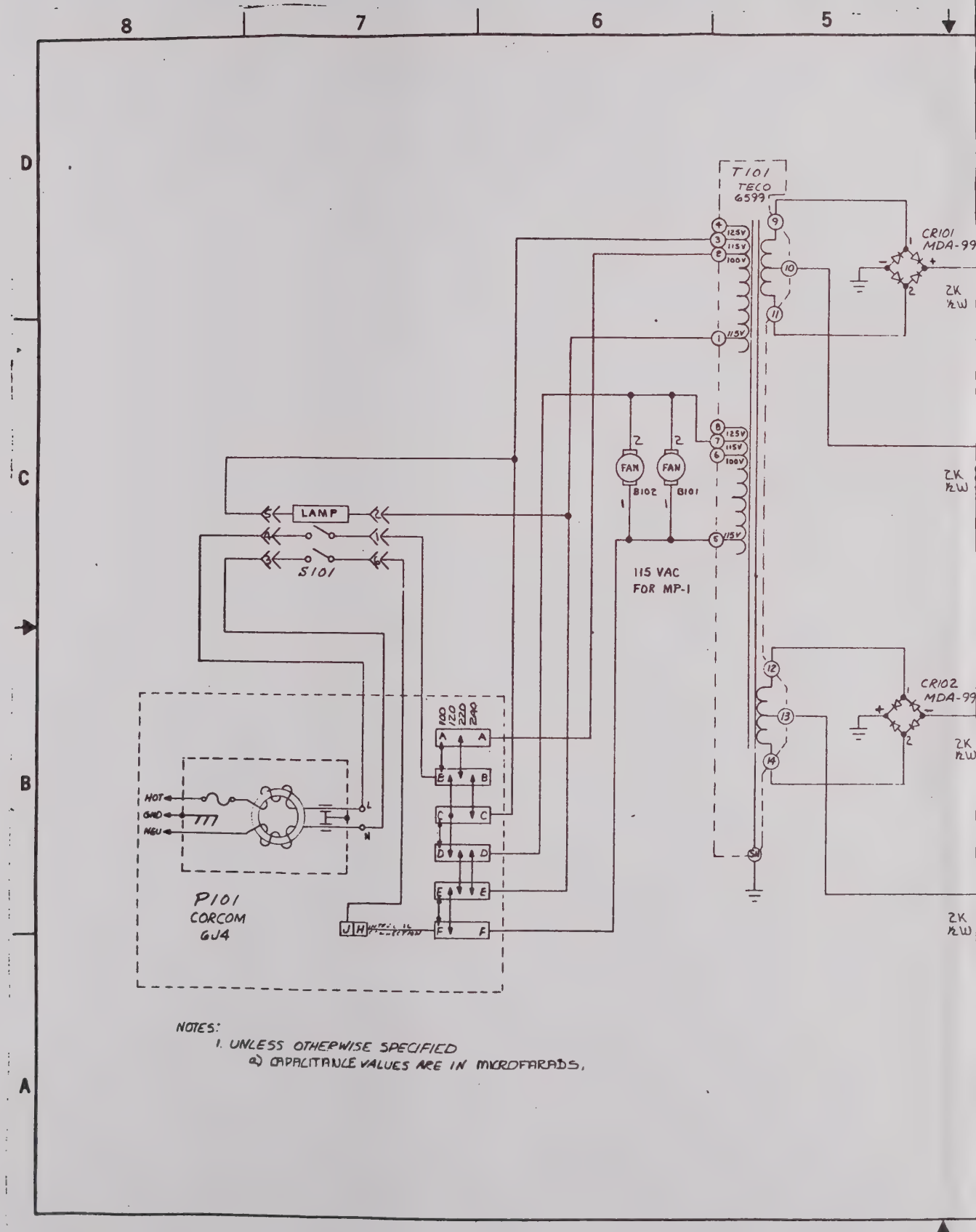
8.1 GENERAL

This section contains Block and Schematic diagrams for the MS-302, MN-302 and MB-302 modules. Figures are given in the table below.

TABLE 8-1

DIAGRAMS

Figure	Description
8.1	MF-5 Power Supply Schematic
8.2	MS-302 Block Diagram
8.3	MS-302 Front-Panel Schematic
8.4	MS-302 Clock Source Schematic
8.5	MS-302 Crystal Oscillator Schematic
8.6	MS-302 Power Supply Schematic
8.7	MS-302 GPIB Adapter Schematic
8.8	MN-302 Block Diagram
8.9	MN-302 Front-Panel Schematic
8.10	MN-302 Code Generator Schematic
8.11	MN-302 Optical Interface Schematic
8.12	MN-302 Power Supply Schematic
8.13	MN-302 GPIB Adapter Schematic
8.14	MB-302 Block Diagram
8.15	MB-302 Front-Panel Schematic
8.16	MB-302 Code ReSync Schematic
8.17	MB-302 BCD Interface Schematic
8.18	MB-302 Counter Board Schematic
8.19	MB-302 Power Supply Schematic
8.20	MB-302 GPIB Adapter Schematic



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   a) CAPACITANCE VALUES ARE IN MICROFARADS.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION	[illegible]	[illegible]
	B	REVISED PER DCN C0865	4/2[illegible]	[illegible]
	C	REVISED PER ECO-01040 [illegible]	12-2-[illegible]	[illegible]
	D	REV PER ECO-01056 R. Nunez 2-10-81	2-11-81	[illegible]

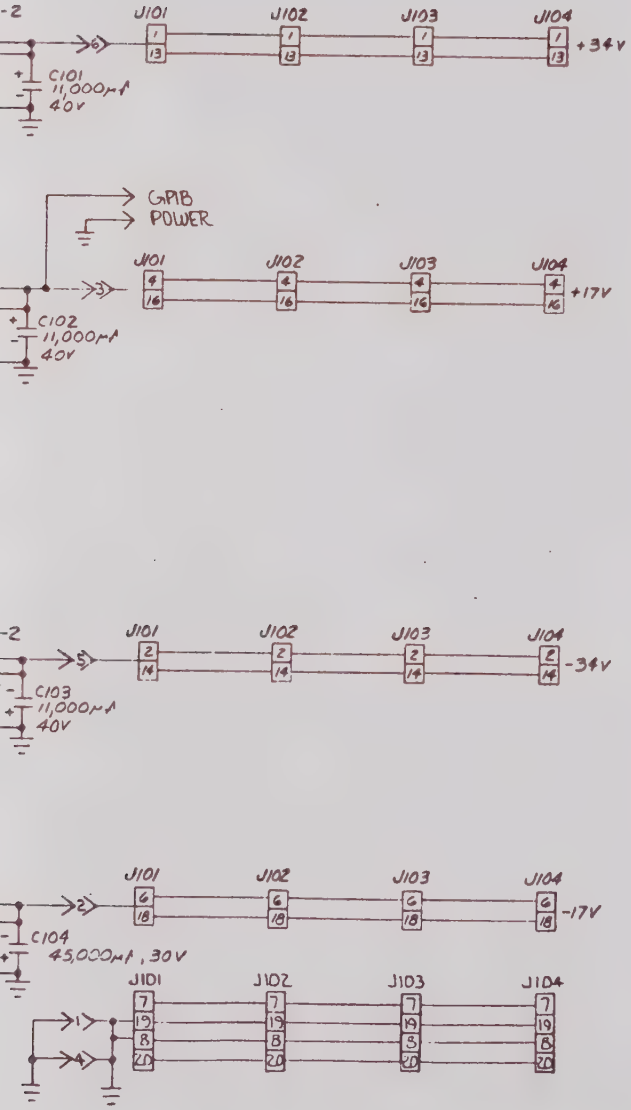
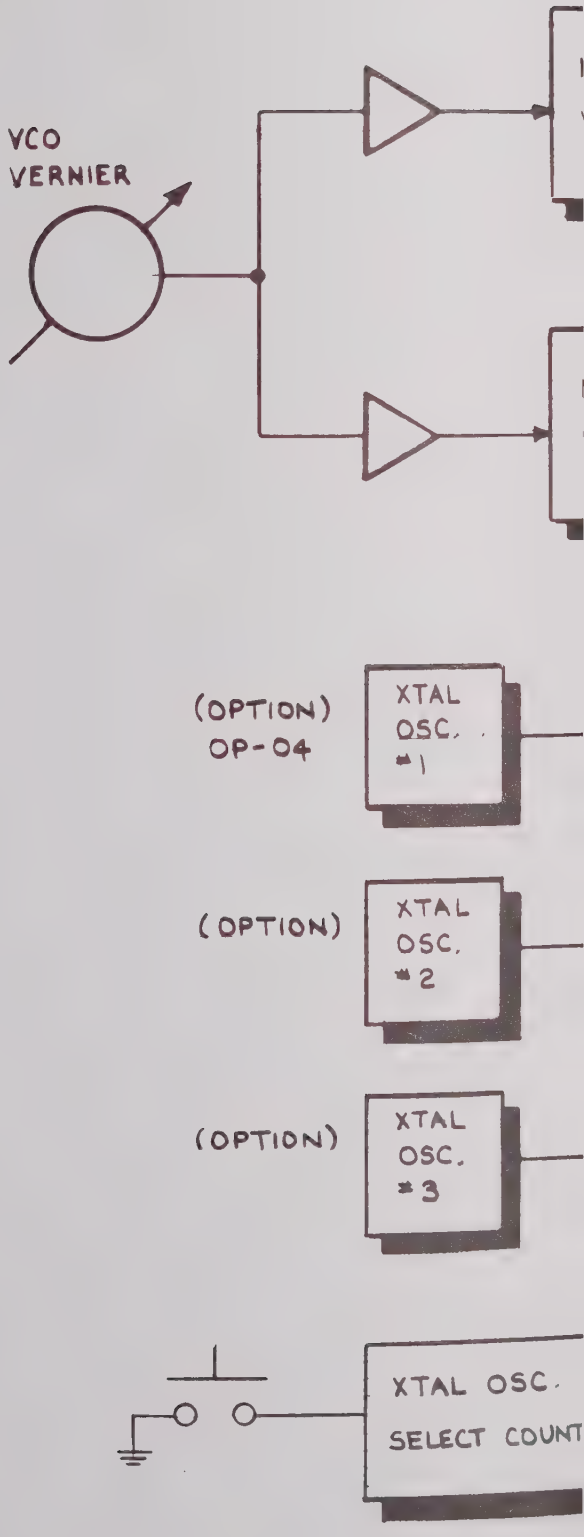
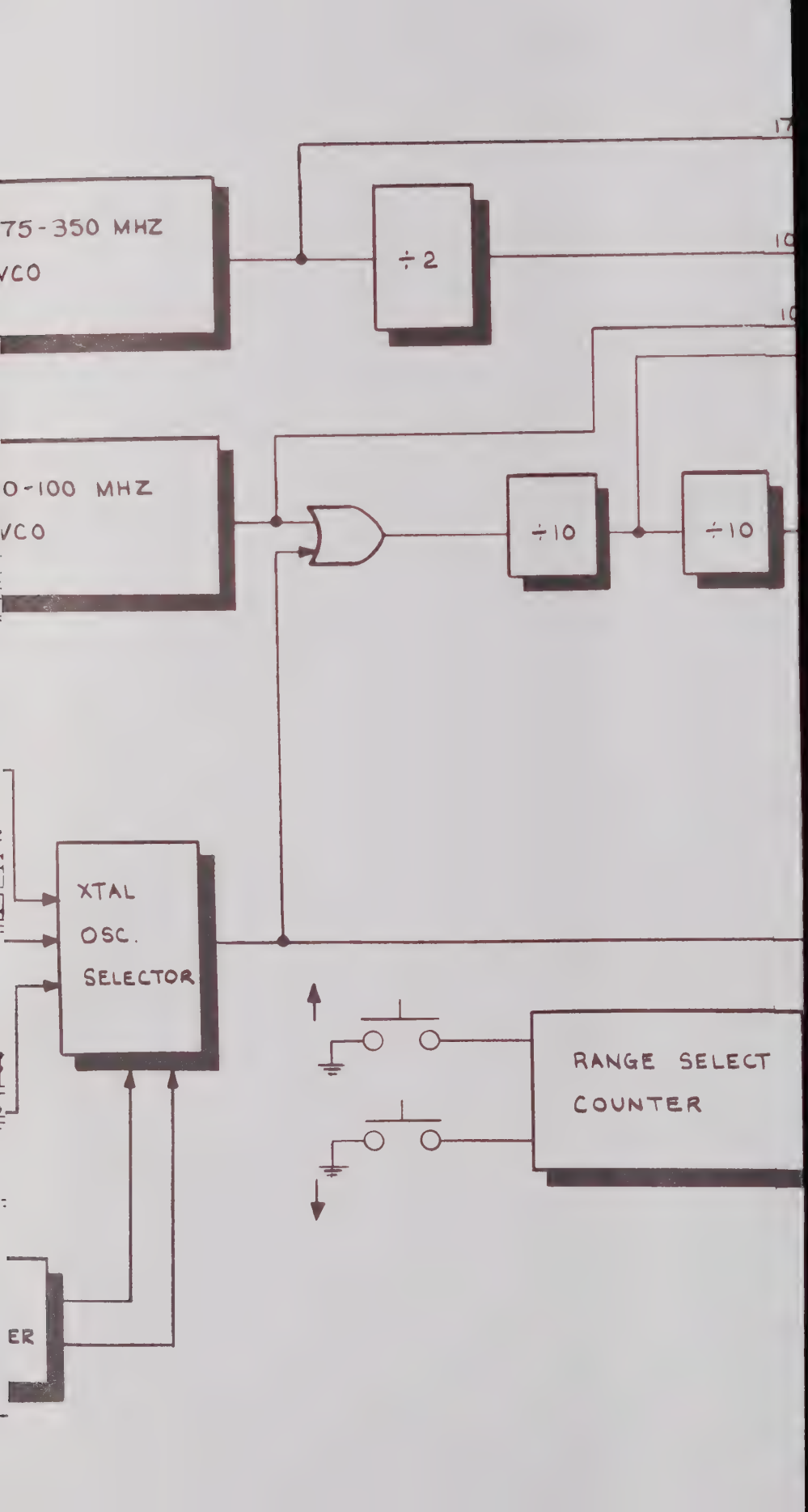


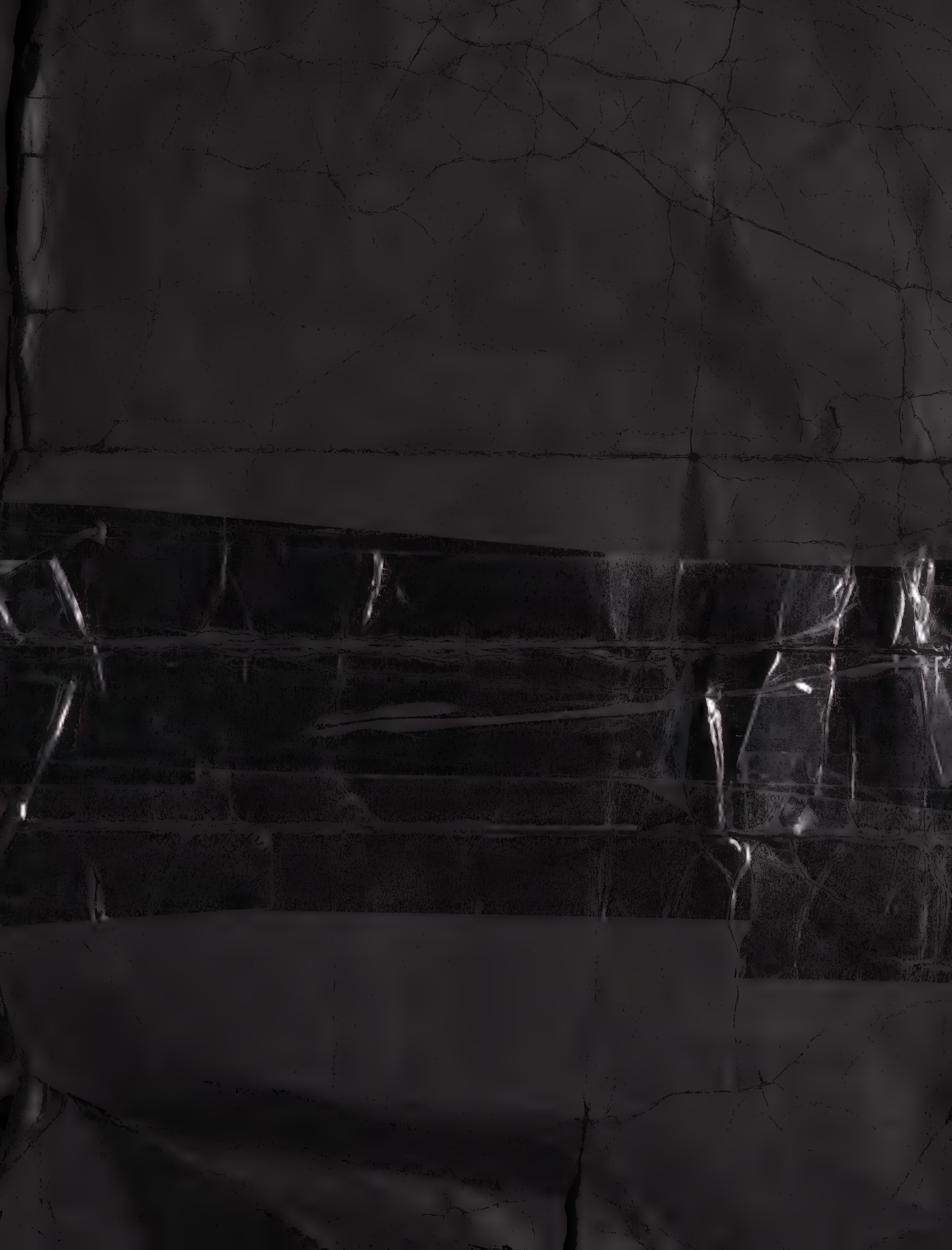
Fig. 8-1
1 of 1

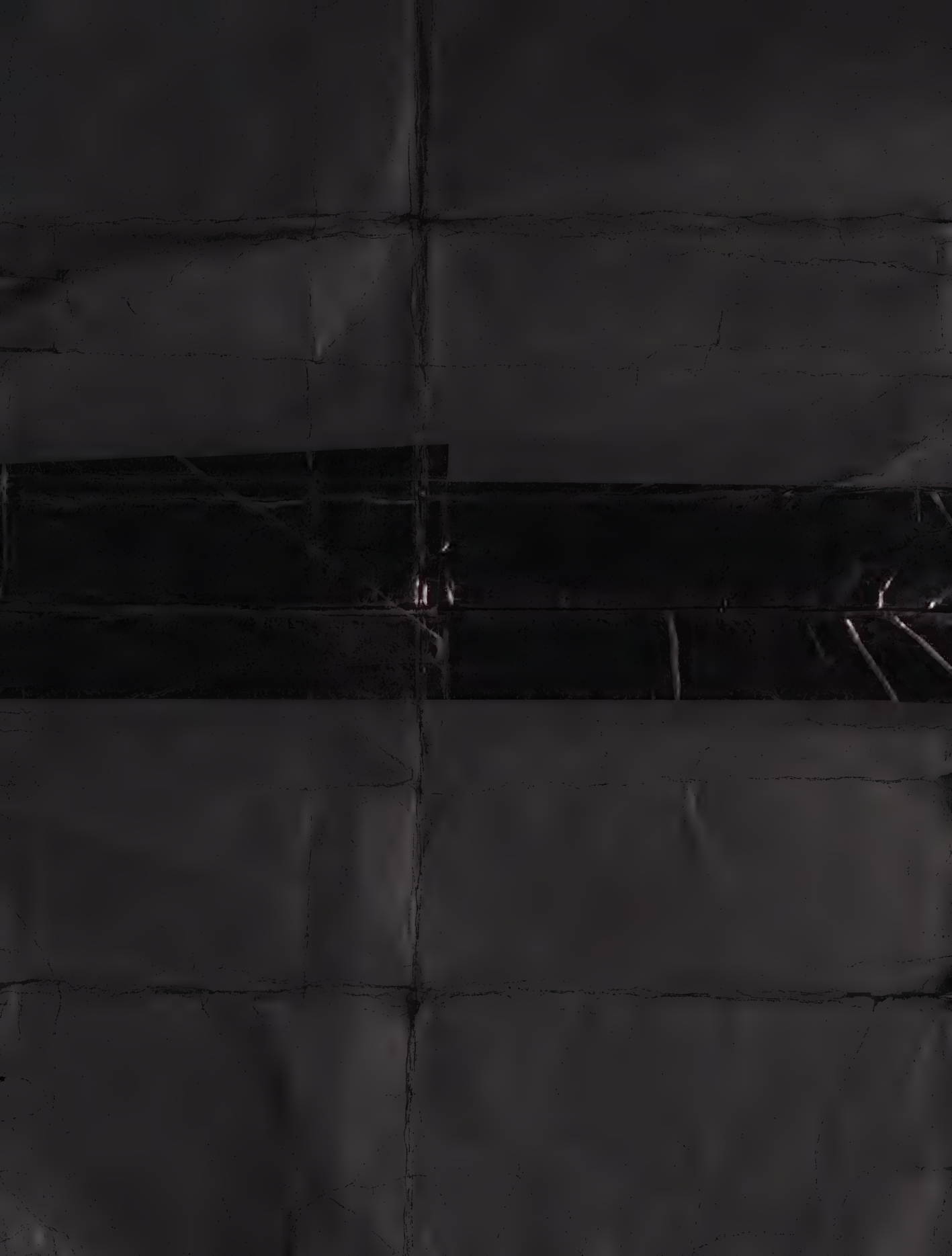
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO. DR 12-10-79 CHK M. Costello	tau-tron inc DRAWING TITLE POWER SUPPLY SCHEMATIC MF-5
NEXT ASSY / USED ON APPLICATION		APPROVED BY DIRECTION OF	SIZE D · CODE IDENT NO. · DRAWING NO. TDJ54336 · REV D SCALE · SHEET 1 OF 1

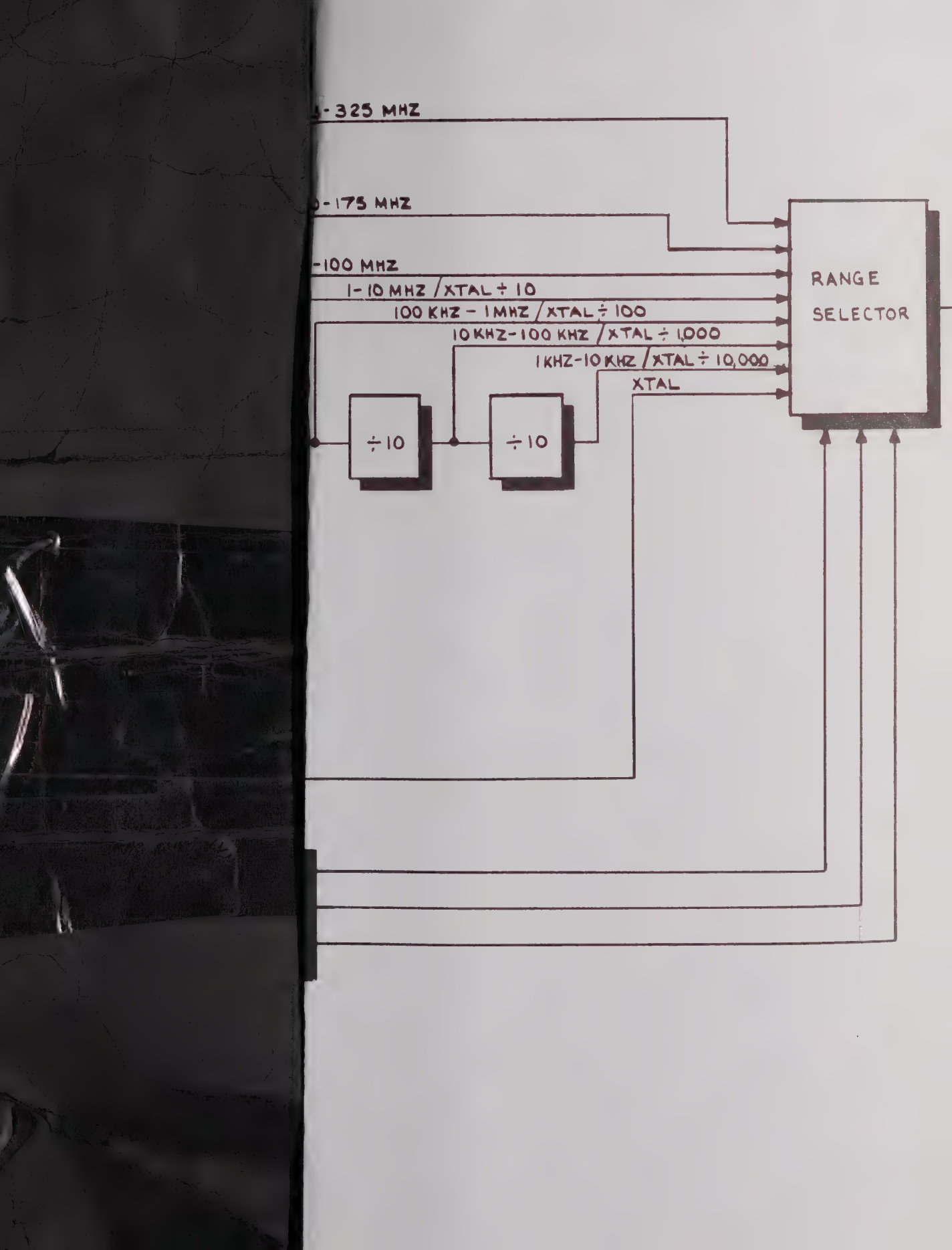
TDJ-54336

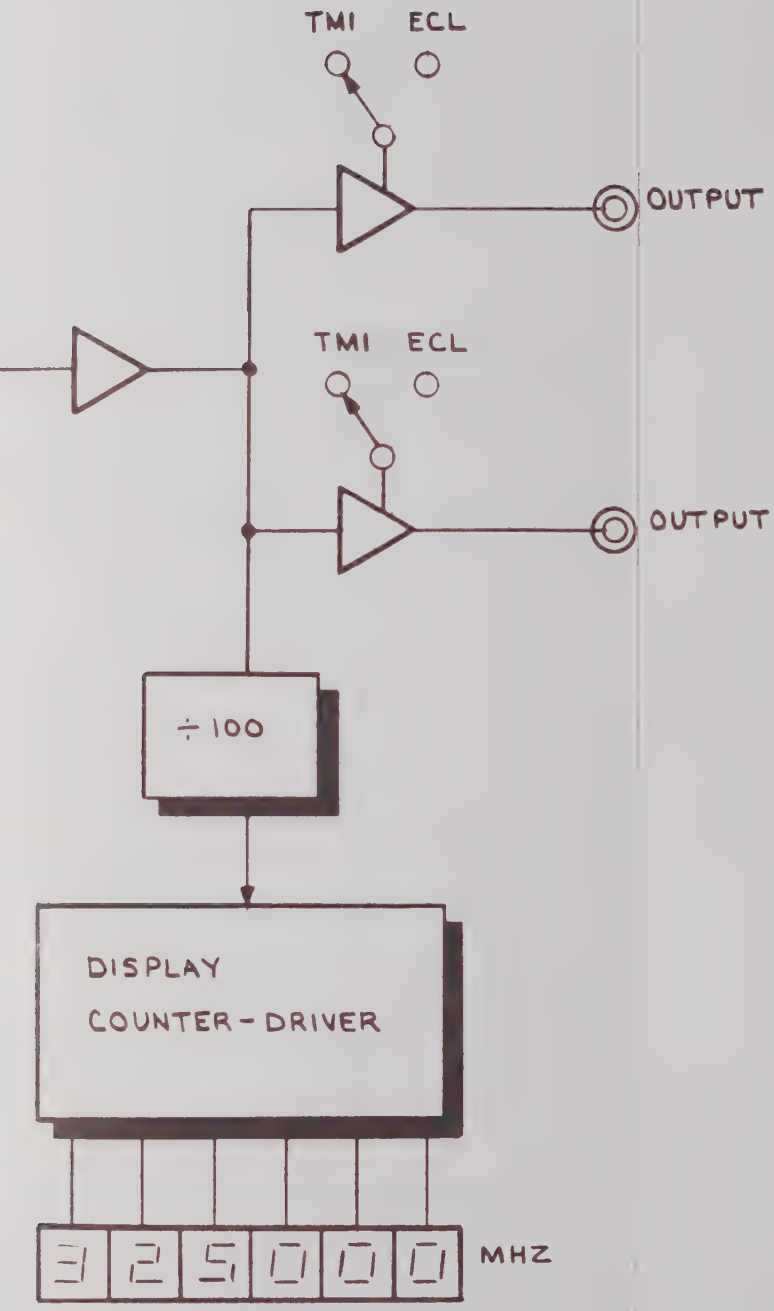

VCO
VERNIER
(OPTION)
OP-04
XTAL
OSC.
#1
(OPTION)
XTAL
OSC.
#2
(OPTION)
XTAL
OSC.
#3
XTAL OSC.
SELECT COUNT


75-350 MHZ
VCO
÷2
0-100 MHZ
VCO
÷10
÷10
XTAL
OSC.
SELECTOR
RANGE SELECT
COUNTER
ER



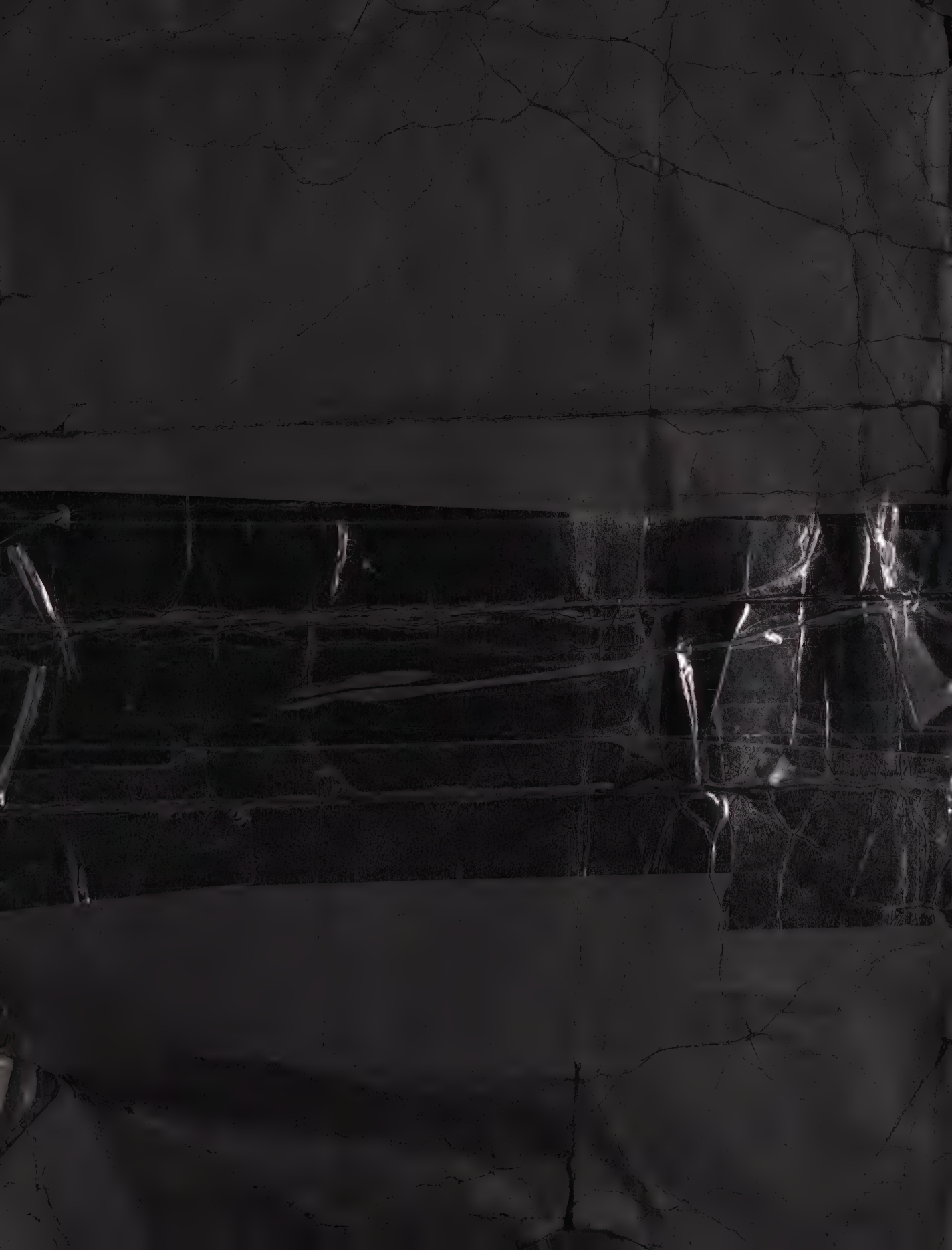


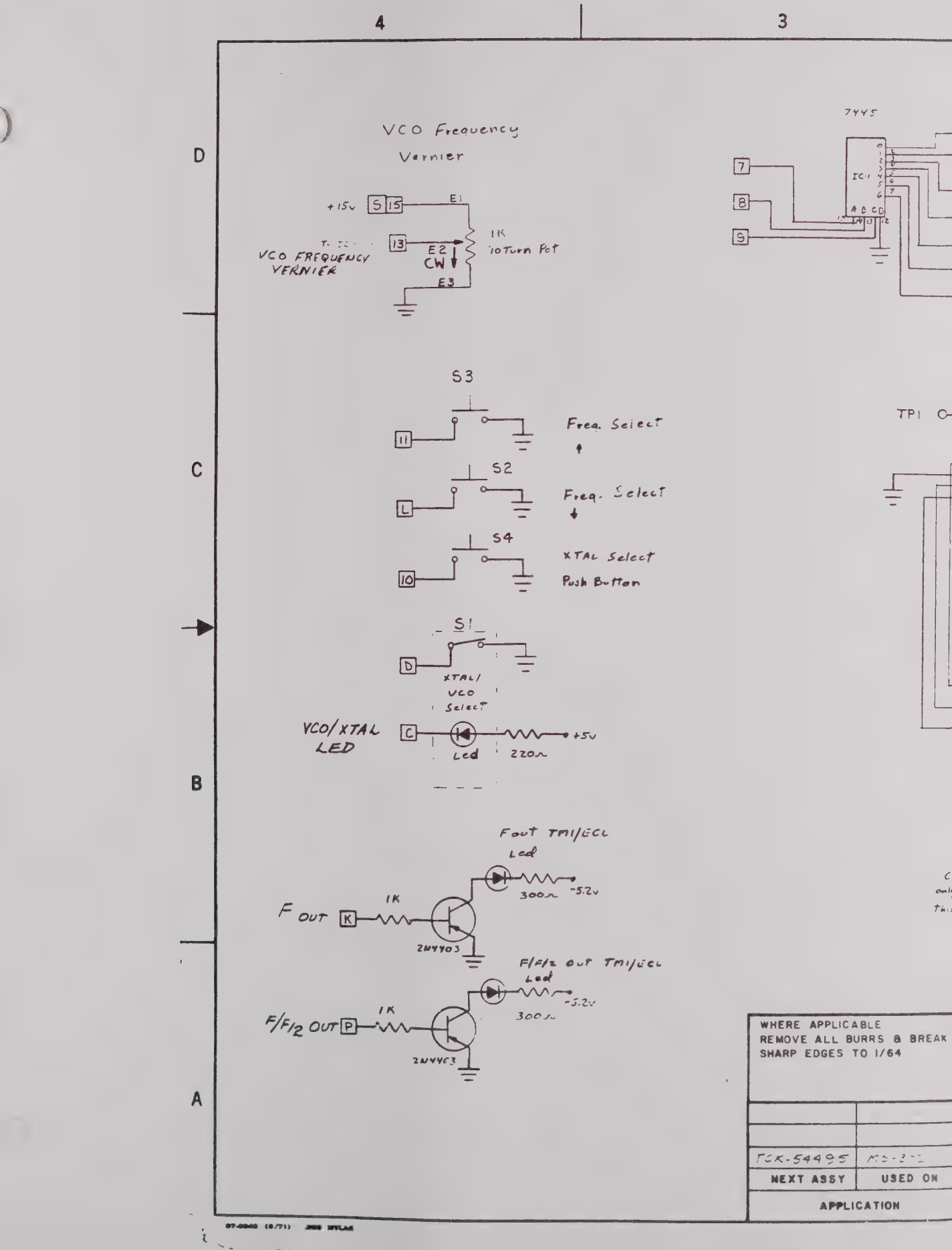

-325 MHZ
-175 MHZ
-100 MHZ
1-10 MHZ / XTAL ÷ 10
100 KHZ - 1MHZ / XTAL ÷ 100
10 KHZ-100 KHZ / XTAL ÷ 1,000
1 KHZ-10 KHZ / XTAL ÷ 10,000
XTAL
÷10
÷10
RANGE
SELECTOR

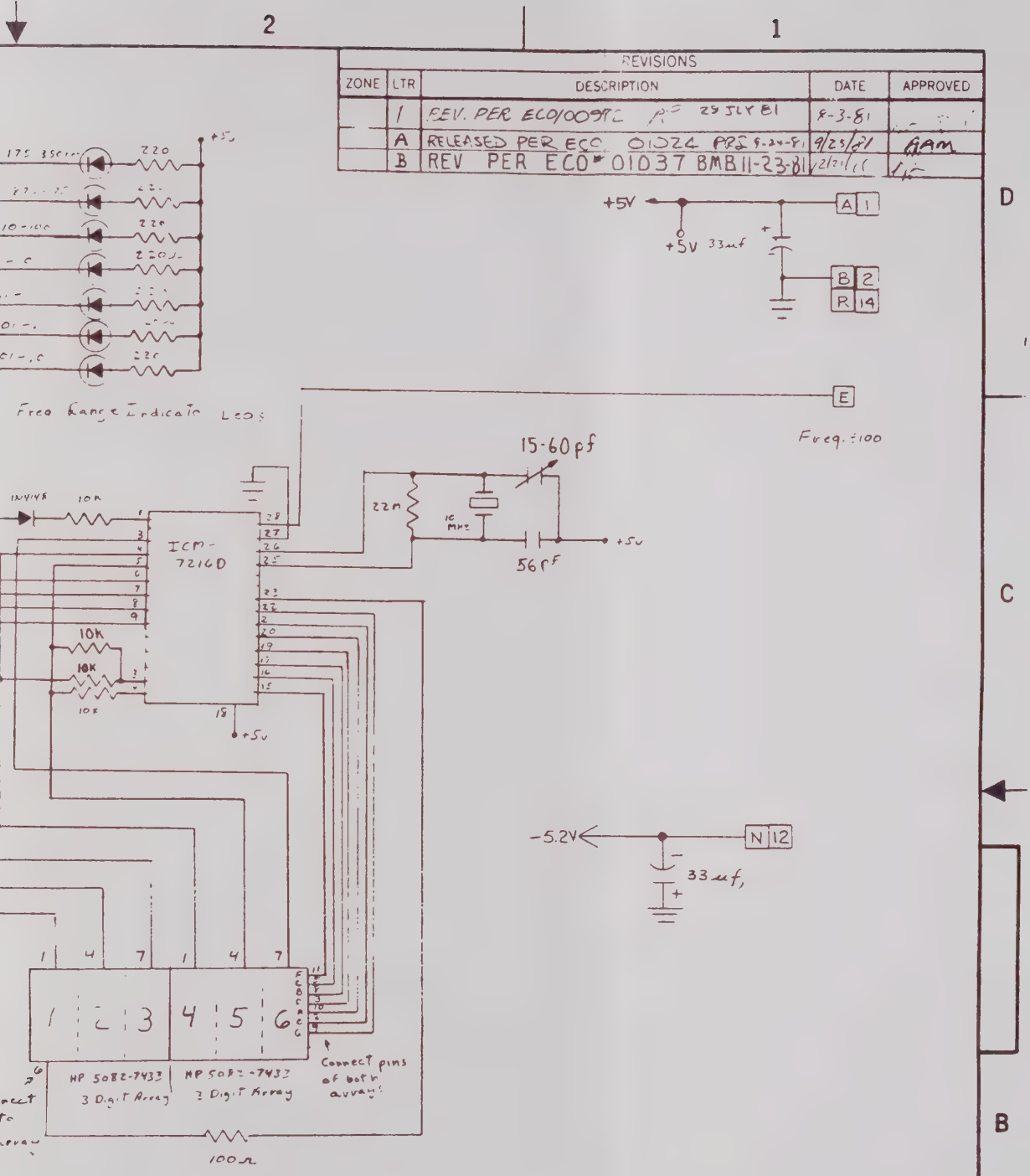


MS-302
BLOCK DIAGRAM

FIG. 8-2
1 of 1

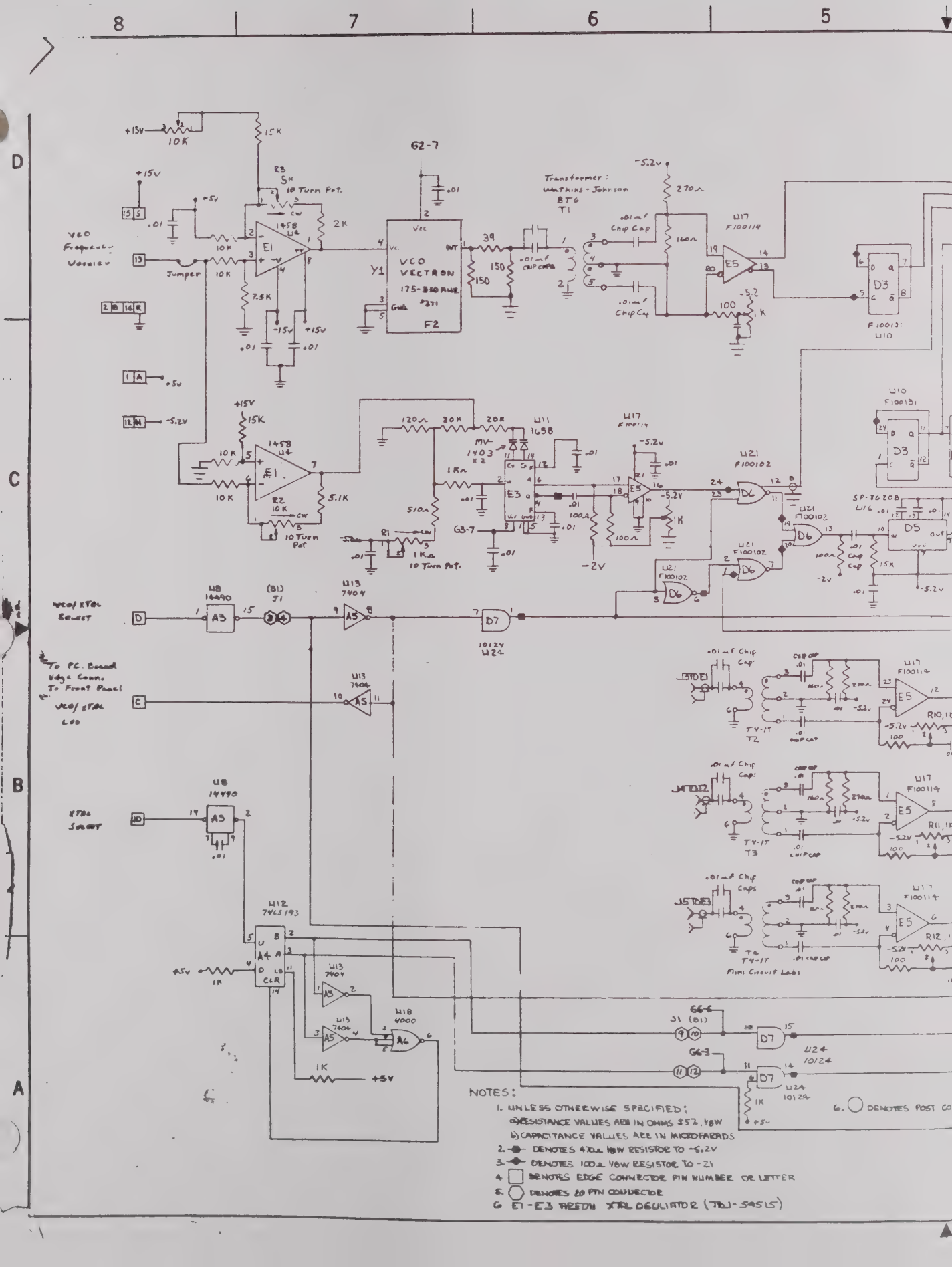



4
3
D
C
B
A
VCO Frequency
Vernier
+15v
S
15
E1
13
E2
CW
E3
1K
10Turn Pot
VCO FREQUENCY
VERNIER
7445
7
8
9
IC-1
A B C D
S3
11
Freq. Select
S2
L
Freq. Select
S4
10
XTAL Select
Push Button
S1
D
XTAL/
VCO
Select
VCO/XTAL
LED
C
Led
220Ω
+5v
TP1
Fout TMI/ECL
Led
300Ω
-5.2v
1K
F OUT
K
2N4403
F/F/2 OUT TMI/ECL
Led
-5.2v
300Ω
1K
F/F/2 OUT
P
2N4403
WHERE APPLICABLE
REMOVE ALL BURRS & BREAK
SHARP EDGES TO 1/64
TCK-54495
NEXT ASSY
USED ON
APPLICATION

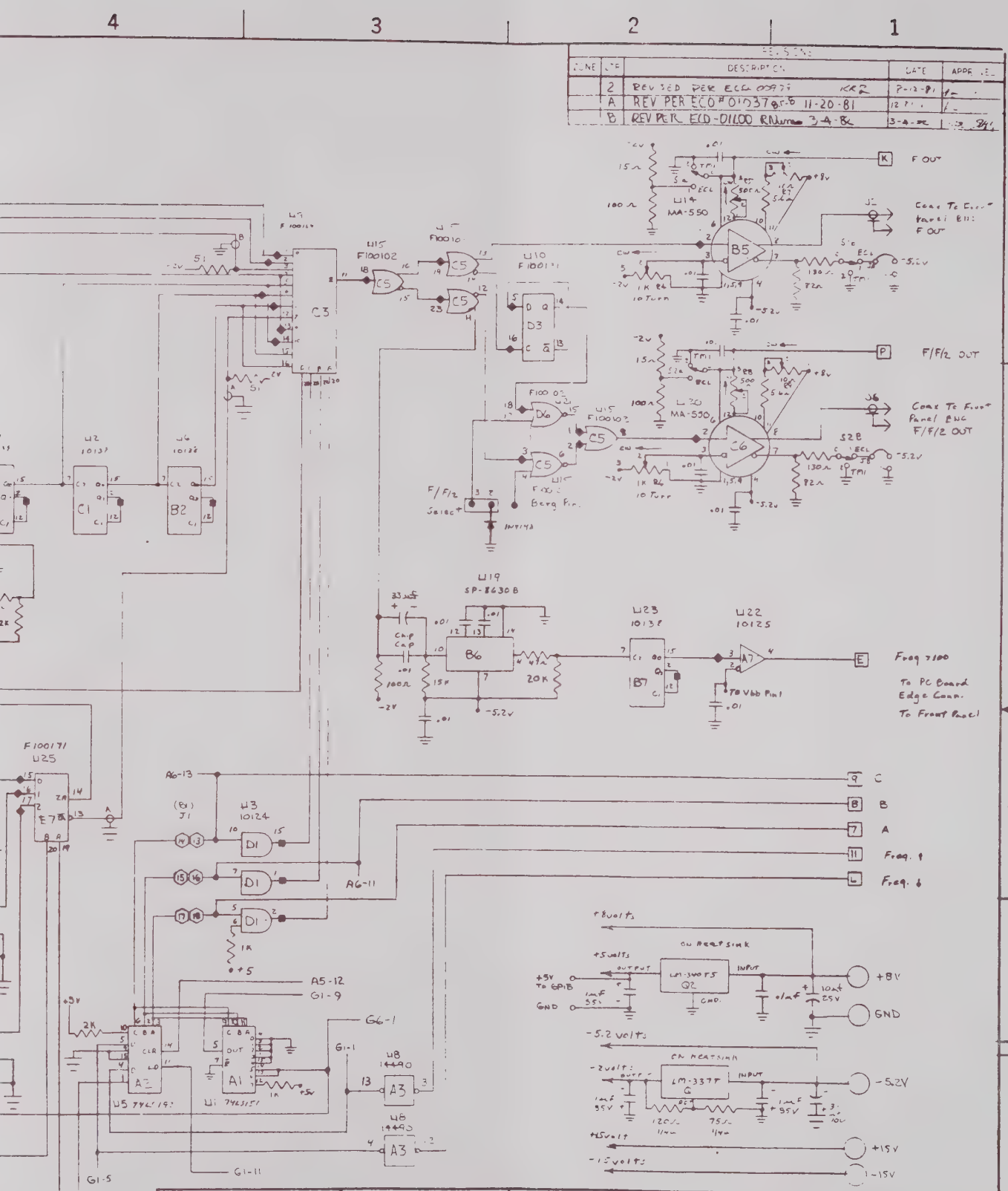


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO.	tau-tron inc	
TOLERANCES: ANGLES ±	DR [illegible]		
FRACTIONS ±	CHK [illegible]	DRAWING TITLE: SCHEMATIC, MS-302 Front Panel	
3 PLACE DECIMALS ±	APPD [illegible]		
2 PLACE DECIMALS ±			
1 PLACE DECIMALS ±			
MATERIAL:	APPROVED	SIZE: -	CODE IDENT NO.
	BY DIRECTION OF	DRAWING NO.: TCJ-54493	REV: B
		SCALE	MS-302 SHEET 1 OF 1

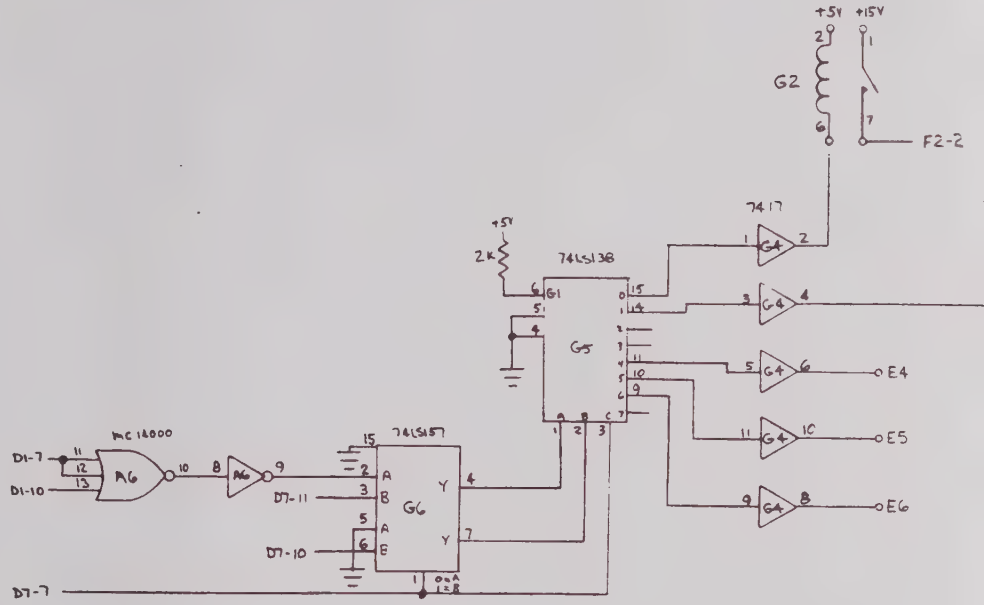
Fig. 8-3
1 of 1

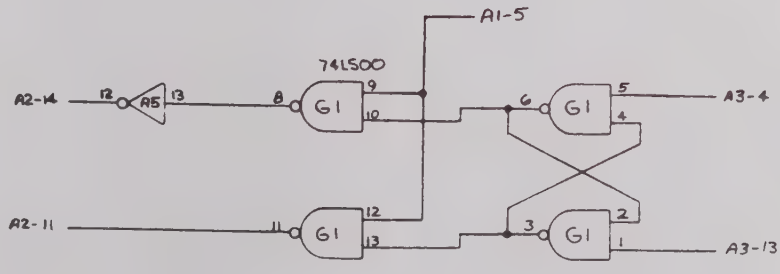

8
7
6
5
D
C
B
A
+15V
10K
15K
R3
5K
10 Turn Pot.
2K
1458
U4
E1
10K
7.5K
.01
-15V
+15V
VCO Frequency Voltage
Jumper
G2-7
Y1
VCO
VECTRON
175-350 MHz
F2
Vcc
OUT
Gnd
39
150
150
.01mf Chip Cap
Transformer:
Watkins-Johnson
BTG
T1
-5.2V
270Ω
160Ω
100
1K
U17
F100114
E5
D3
F10013:
U10
U10
F100131
+5V
-5.2V
120Ω
20K
20K
U11
1658
MV
1403
x2
1KΩ
5.1K
R2
10K
10 Turn Pot
R1
1KΩ
10 Turn Pot.
G3-7
E3
100Ω
-2V
U21
F100102
D6
D5
SP-8620B
U16
15K
U8
14490
A3
(B1)
J1
U13
7404
A5
D7
10124
U24
VCO/XTAL Select
To PC. Board Edge Conn. To Front Panel
VCO/XTAL LOD
J5TDE1
J4TDE2
J3TDE3
TY-1T
T2
T3
T4
Mini Circuits Labs
R10,
R11,
R12,
XTAL Select
U12
74LS193
A4
A
B
U
D
LD
CLR
A6
U18
4000
1K
+5V
G6-6
G6-3
J1 (B1)
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE VALUES ARE IN OHMS ±5%, ¼W
b) CAPACITANCE VALUES ARE IN MICROFARADS
2. DENOTES 470Ω ¼W RESISTOR TO -5.2V
3. DENOTES 100Ω ¼W RESISTOR TO -2V
4. DENOTES EDGE CONNECTOR PIN NUMBER OR LETTER
5. DENOTES 20 PIN CONNECTOR
6. E1-E3 AREON XTAL OSCILLATOR (TRW-59515)
6. DENOTES POST CO

ZONE	LTR	DESCRIPTION	DATE	APPR
	2	REVISED PER ECO 00975 KR2	7-12-81	
	A	REV PER ECO # 01037 & -D 11-20-81	12	
	B	REV PER ECO-01100 RNums 3-4-82	3-4-82	



WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR CHK APPD APPROVED BY DIRECTION OF	tau-tron inc DRAWING TITLE SCHEMATIC CLOCK SOURCE Fig. 8-4 1 of 2
TDR-54514 / MS-302 NEXT ASSY / USED ON APPLICATION			SIZE D / CODE IDENT NO / DRAWING NO. TDW-54512 / REV E SCALE ¼ / SHEET 1 OF 2


+5V
+15V
G2
F2-2
7417
+5V
2K
74LS138
G1
G5
G4
E4
E5
E6
MC 12000
D1-7
D1-10
A6
D7-11
D7-10
D7-7
74LS157
G6
A
B
Y


A1-5
74LS00
A2-14
A5
G1
A3-4
A2-11
A3-13

4 3 2 1

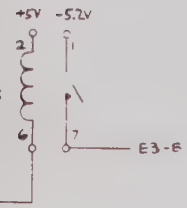
ZONE	LTR	DESCRIPTION	DATE	APPR'D
		SEE SH 1 FOR REVISIONS		

D

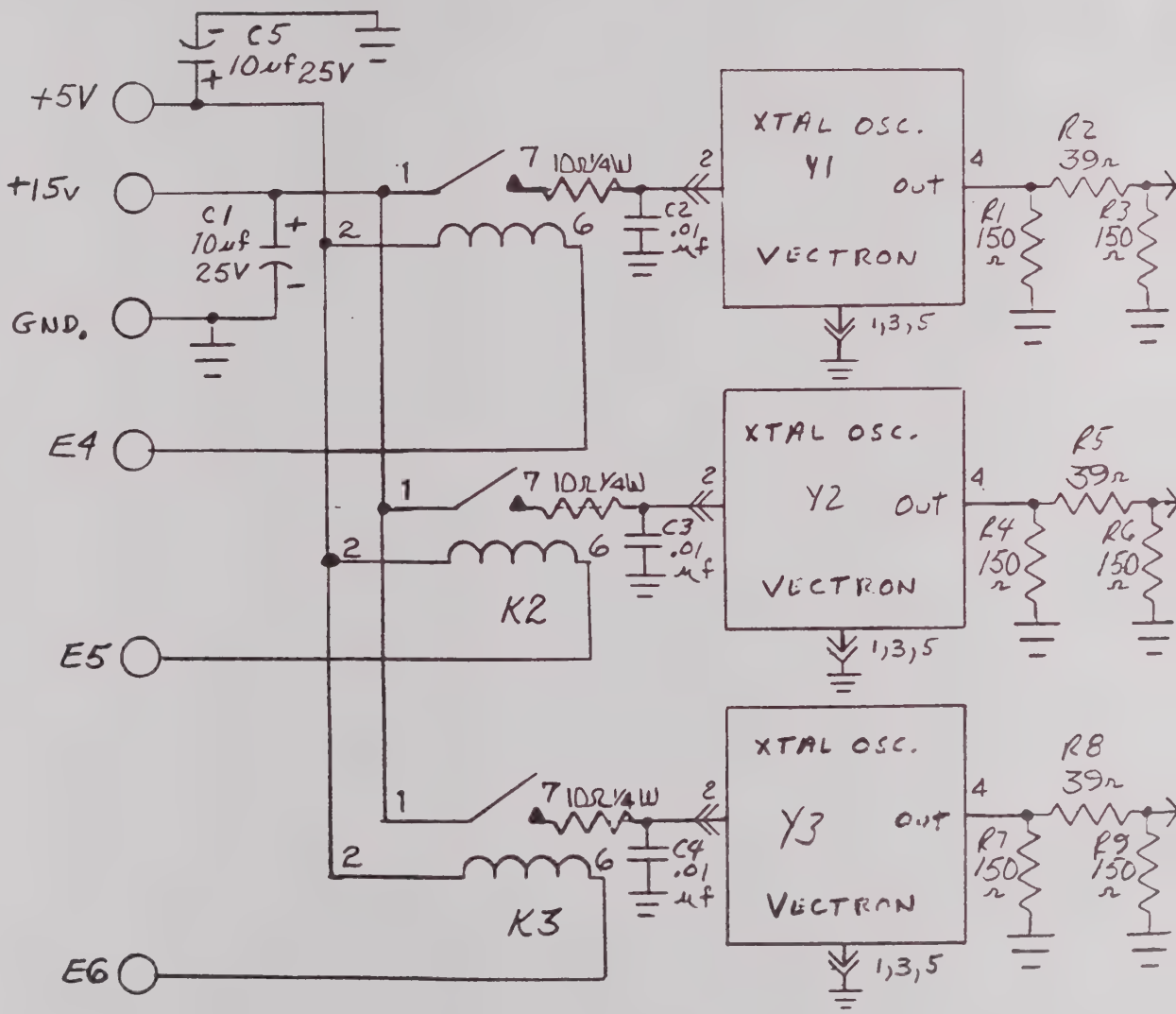
C

B

A



WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO	tau-tron INC
	TOLERANCES ANGLES ±	DR [illegible] 8-11-81	
	FRACTIONS ±	CHK [illegible] 8-11-81	DRAWING TITLE
	3 PLACE DECIMALS ±	APPD	SCHEMATIC CLOCK SOURCE — Fig. 8-4 2 of 2
	2 PLACE DECIMALS ±		
	1 PLACE DECIMALS ±		
NEXT ASSY / USED ON	MATERIAL	APPROVED	SIZE: D | CODE IDENT NO | DRAWING NO: TDJ-54512 | REV: B
APPLICATION		BY DIRECTION OF	SCALE: None | MS-202 | SHEET 2 OF 2



WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.	
	MS-302
NEXT ASSY	USED ON
APPLICATION	

07-0013 (6-71)

3	2	1

REVISIONS					
ZONE	LTR	DESCRIPTION	DATE	APPROVED	
	0	ORIGINATED	4-27-81		
	1	UPDATED PROTOTYPE JJ 4-29-81	5-11-81	[illegible]	[illegible]
	2	REV PER ECO/00979 [illegible] 29JLY81	8-4-81	[illegible]	DAP
	A	REV PER ECO-01130 RBurns 3-4-82	3-4-82	BUDD	[illegible]

D

E1 TO J3

C

E2 TO J4

NOTES:

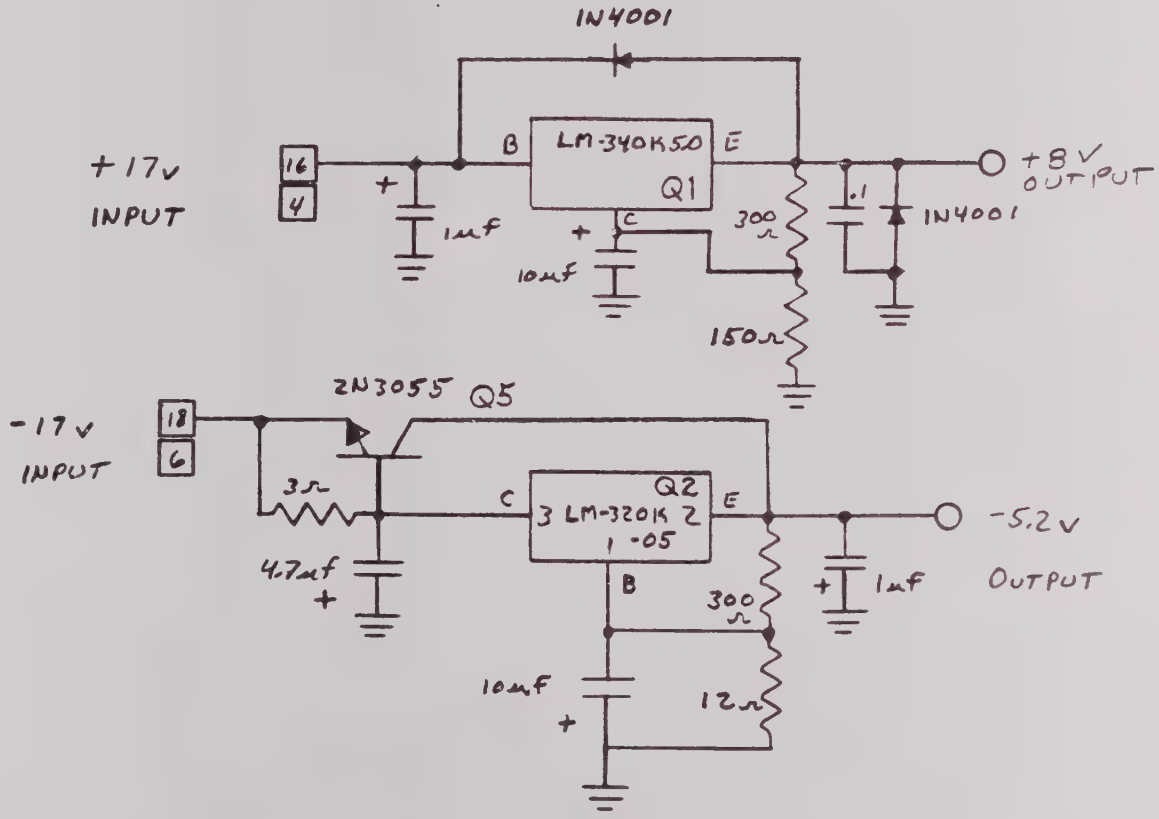
1. COAX HARD SOLDERED TO PC BOARD (3 PLACES)
2. J3 - J5 ON CLOCK SOURCE (TBJ-54512)

E3 TO J5

B

A

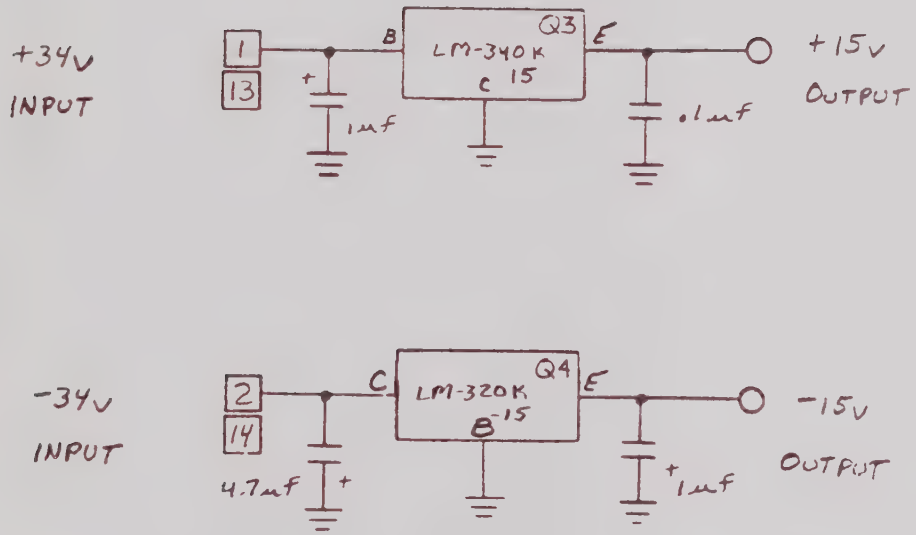
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO. DR S.A. McLeod 4/27/81 CHK [illegible] 5-11-81 APPD [illegible] 5-11-81 APPROVED BY DIRECTION OF	tau-tron inc DRAWING TITLE SCHEMATIC XTAL OSCILLATOR Fig. 8-5 1 of 1 SIZE B | CODE IDENT NO. | DRAWING NO. TBJ-54515 | REV A SCALE ~ | MS-302 | SHEET 1 OF 1	



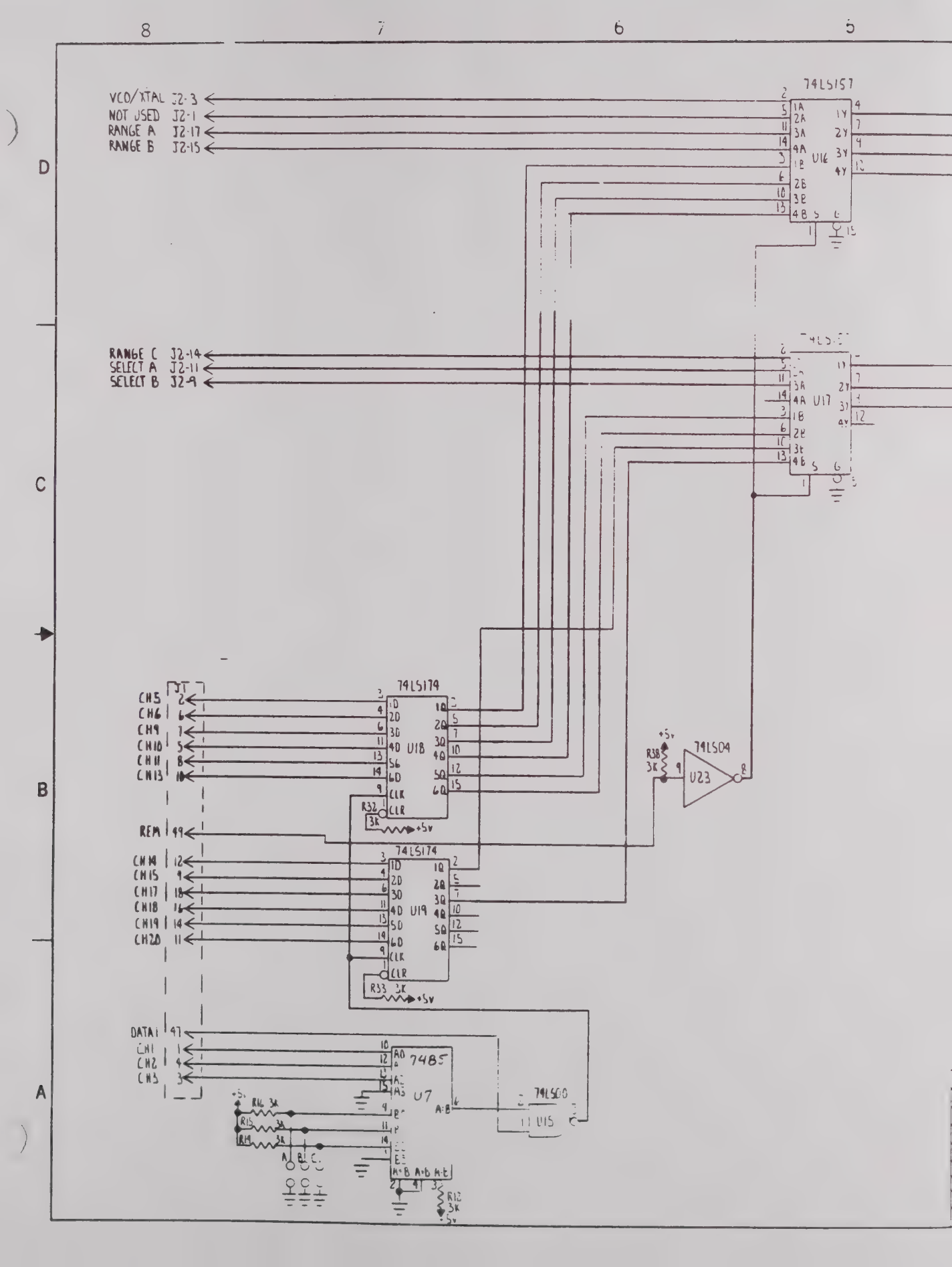
WHERE APPLICABLE: REMOVE ALL BURRS & BREA SHARP EDGES TO 1/64.	
NEXT ASSY	USED ON
APPLICATION	

07-0013 16-711

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	UPDATED PROTOTYPE ECO/CO979 29JUL81	8-3-81	[illegible]
	A	ECO # 01024	9-25-81	AAM

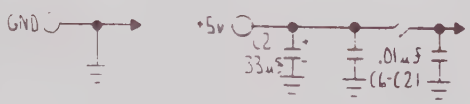


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ±	CONTR NO.		tau-tron inc
	DR SAM	9-27-81	
	CHK		DRAWING TITLE: MS-302 Power Supply — Fig. 8-6 1 of 1
	APPD		
MATERIAL:	APPROVED		SIZE B / CODE IDENT NO. / DRAWING NO. TBJ-54511 / REV A
	BY DIRECTION OF		SCALE — / SHEET 1 OF 1


8
7
6
5
D
C
B
A
VCO/XTAL J2-3
NOT USED J2-1
RANGE A J2-17
RANGE B J2-15
74LS157
U16
RANGE C J2-14
SELECT A J2-11
SELECT B J2-9
U17
J1
CH5
CH6
CH9
CH10
CH11
CH13
74LS174
U18
REM
CH14
CH15
CH17
CH18
CH19
CH20
U19
R32 3k
R33 3k
+5v
74LS04
U23
R38 3K
DATA1
CH1
CH2
CH3
7485
U7
74LS00
U15
R14 3k
R15 3k
R16 3k
A=B A>B A<B
R12 3k

	REVISED ECO#00943, JRP 17-JUN 81	6-18-81	RJL
E	REDRAWN BMD. 5-18-82	5-18-82	PA

J2-4 VCO/XTAL
J2-2 NOT USED
J2-18 RANGE A
J2-16 RANGE B
J2-13 RANGE C
J2-12 SELECT A
J2-10 SELECT B



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE VALUES ARE IN OHMS' 1/8W ±5%
   B) CAPACITANCE VALUES ARE IN MICROFARADS

Fig. 8-7
1 of 1

REFERENCE DESIGNATIONS	
ST USED	UNUSED
4	R13
7	
2	

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

CONTR N.
DES A. PERLMUTTER 2/3/82
CHK [illegible] PER 4/[illegible]/82
APP C PERLMUTTER [illegible]
APPROVED
BY DIRECTION OF

tau-tron inc

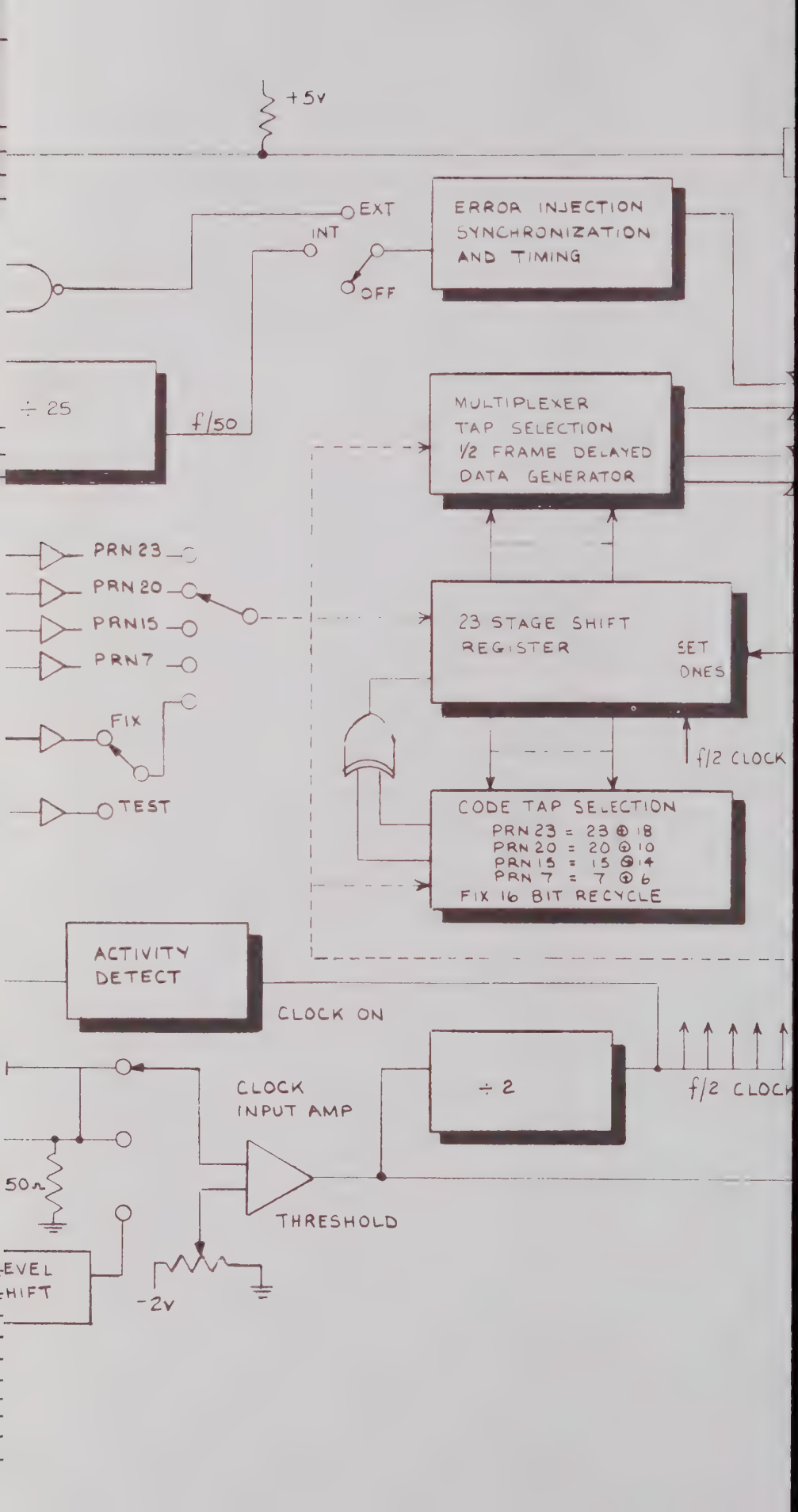
DRAWING TITLE
SCHEMATIC
MS-302
TMI MODULE GPIB ADAPTOR

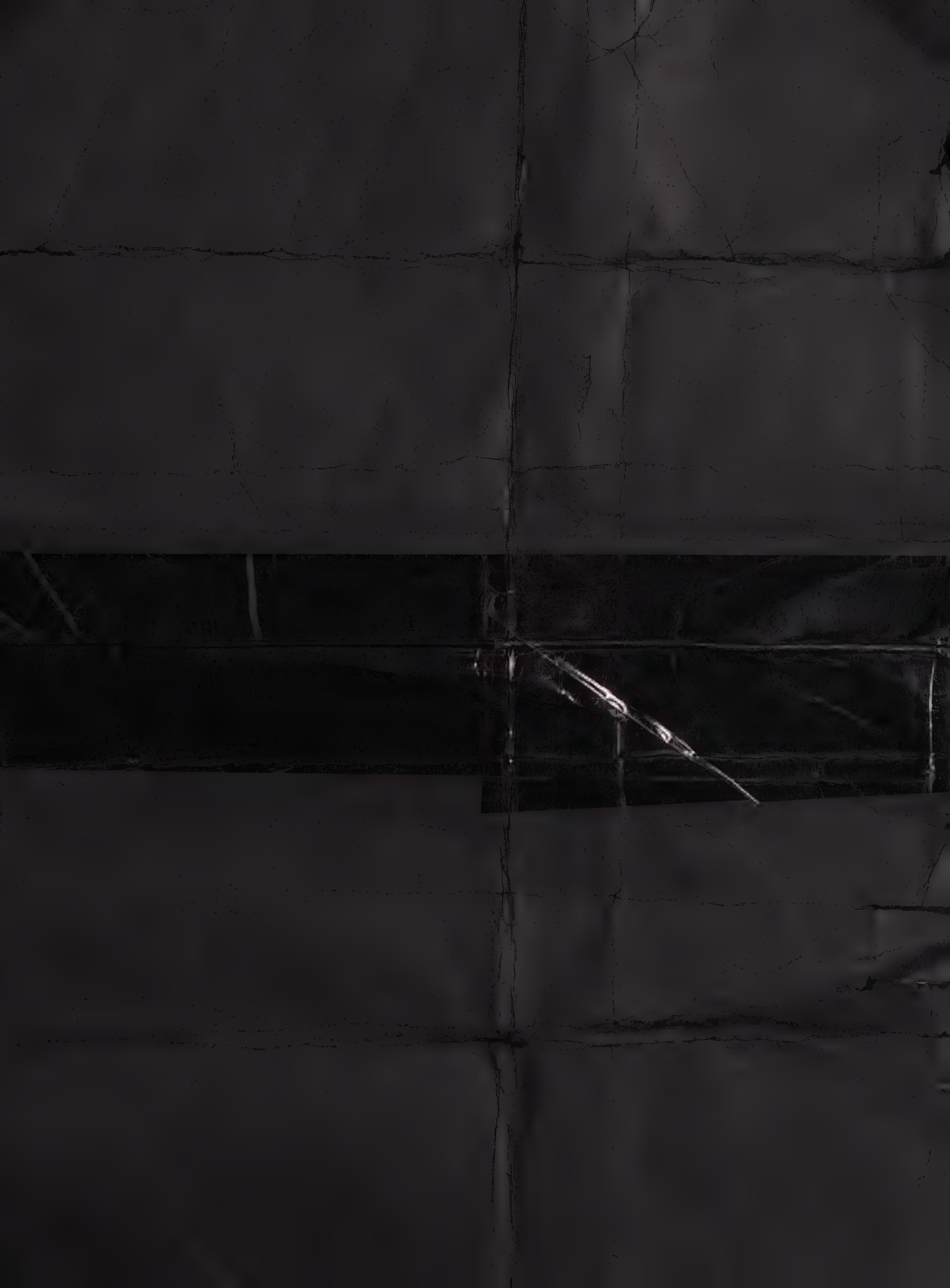
D-54541	MS-302
NEXT ASSY	USED ON
APPLICATION	

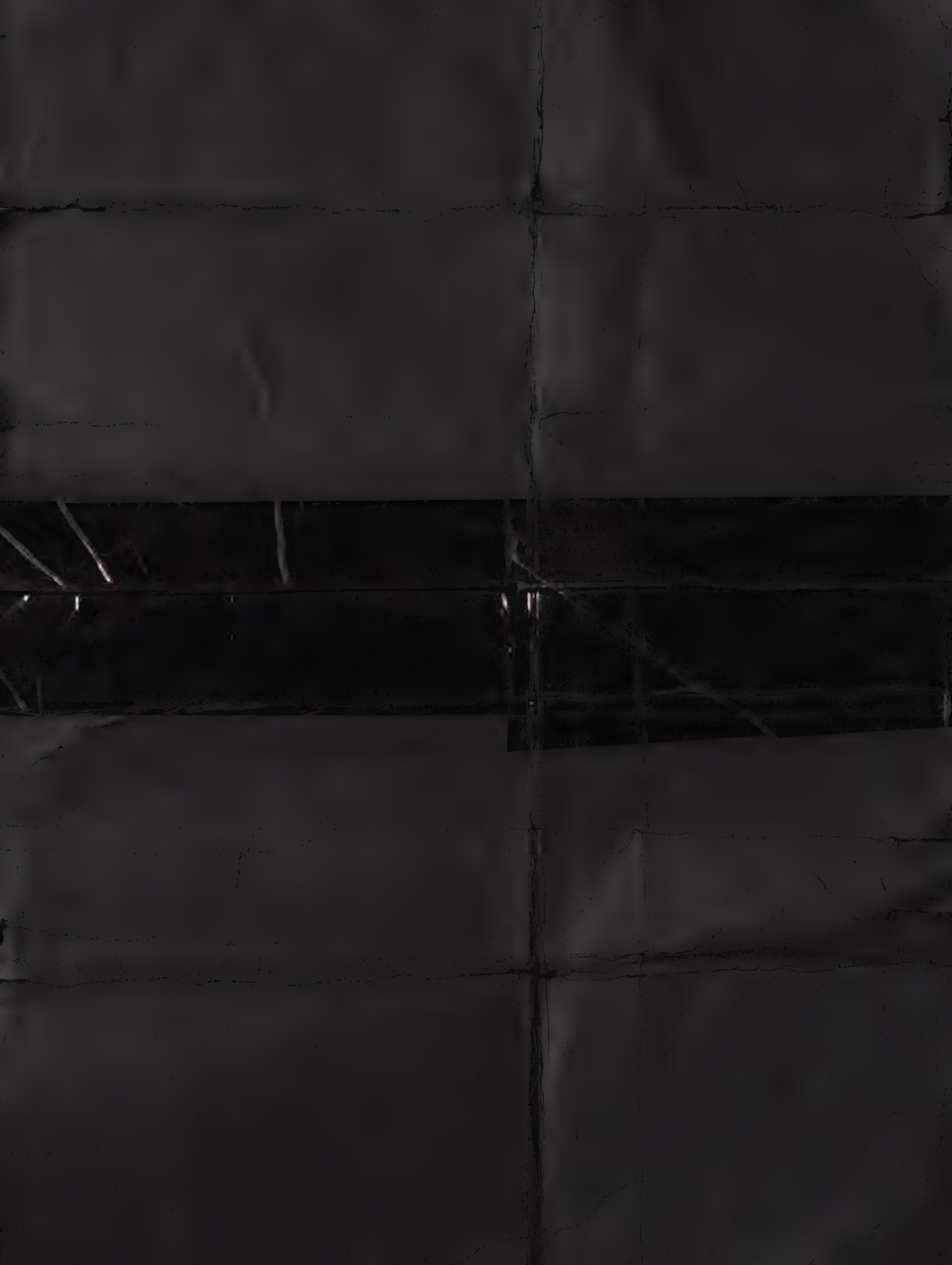
SIZE | CODE IDENT NO | DRAWING NO | REV
D | D-54540 | E

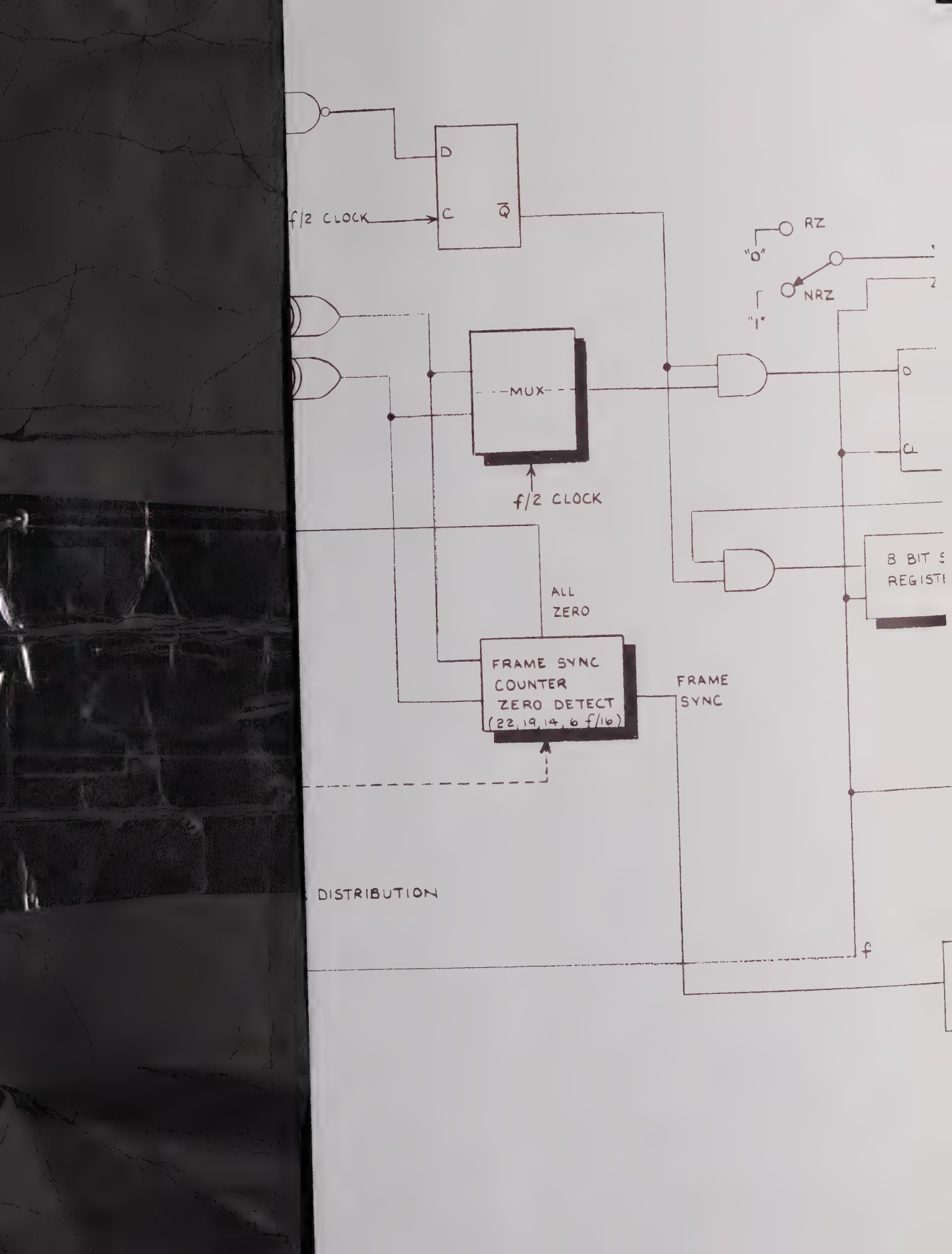
SCALE | TMI [illegible] | SHEET 1 OF

DATA
INHIBIT
+5V
EXT
ERROR
INJECT
f/2 CLOCK
CLOCK
IN
AC
325 MHZ
TMI
ECL
50Ω
-2V


+5v
EXT
INT
OFF
ERROR INJECTION
SYNCHRONIZATION
AND TIMING
÷ 25
f/50
MULTIPLEXER
TAP SELECTION
1/2 FRAME DELAYED
DATA GENERATOR
PRN 23
PRN 20
PRN 15
PRN 7
FIX
TEST
23 STAGE SHIFT
REGISTER
SET
ONES
f/2 CLOCK
CODE TAP SELECTION
PRN 23 = 23 ⊕ 18
PRN 20 = 20 ⊕ 10
PRN 15 = 15 ⊕ 14
PRN 7 = 7 ⊕ 6
FIX 16 BIT RECYCLE
ACTIVITY
DETECT
CLOCK ON
CLOCK
INPUT AMP
÷ 2
f/2 CLOCK
50Ω
THRESHOLD
-2v






D
C
Q
f/2 CLOCK
RZ
"0"
NRZ
"1"
MUX
f/2 CLOCK
D
CL
8 BIT S
REGISTI
ALL
ZERO
FRAME SYNC
COUNTER
ZERO DETECT
(22, 19, 14, 6 f/16)
FRAME
SYNC
DISTRIBUTION
f

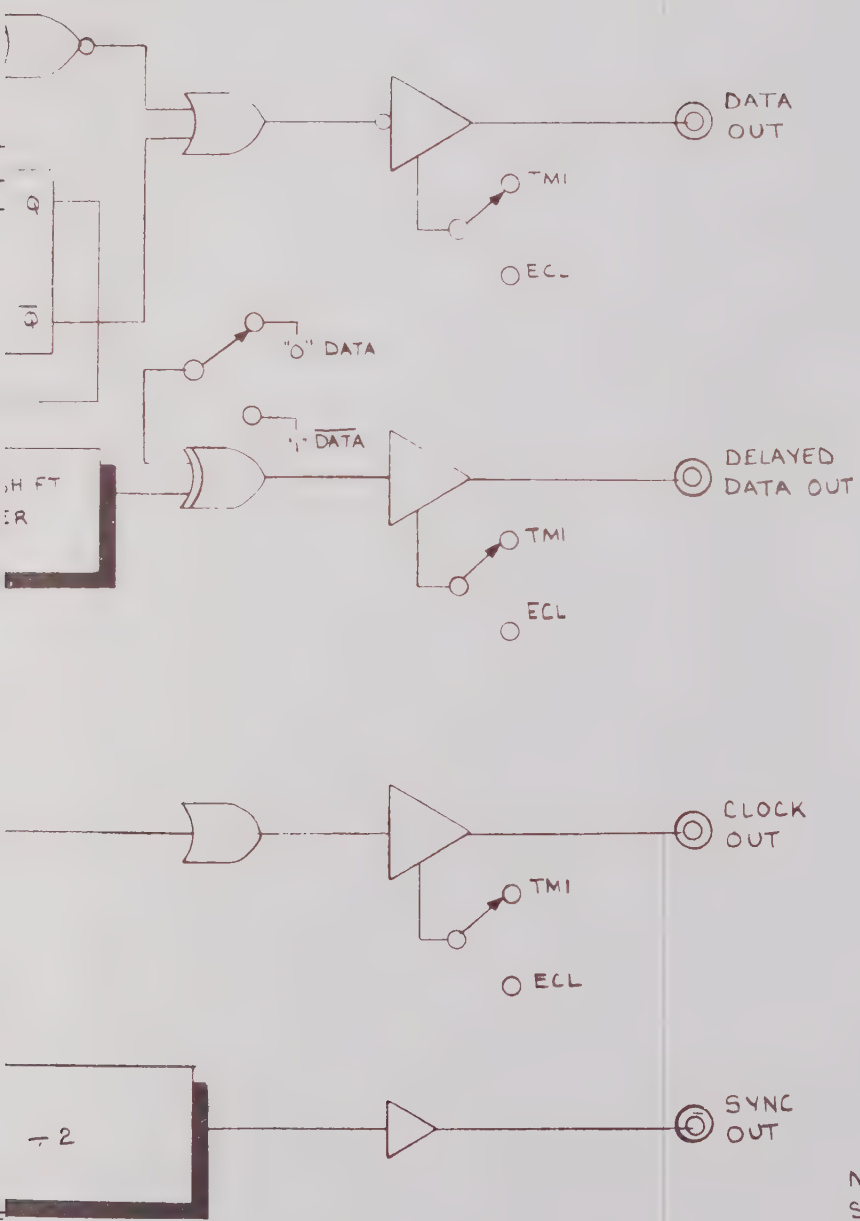
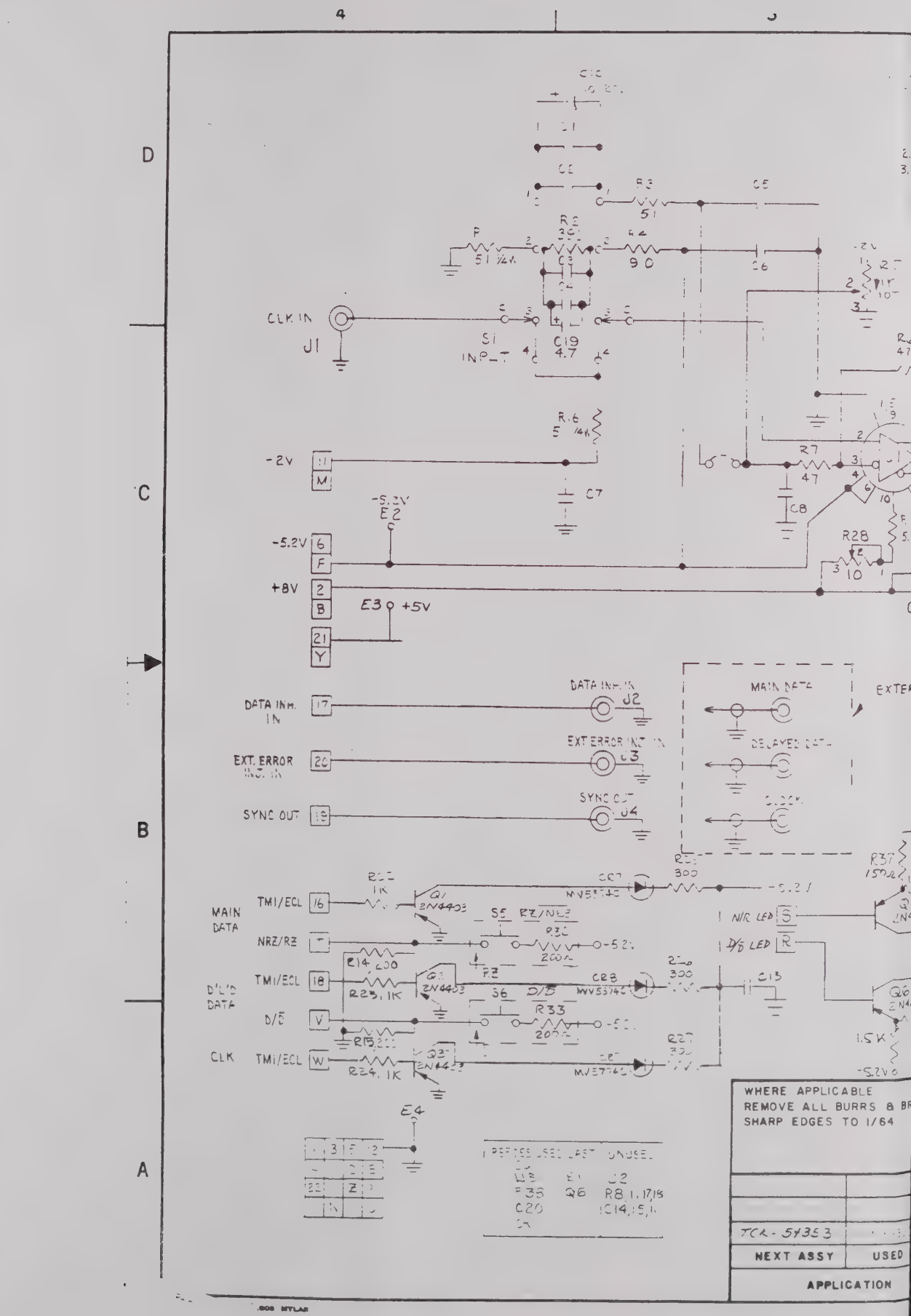
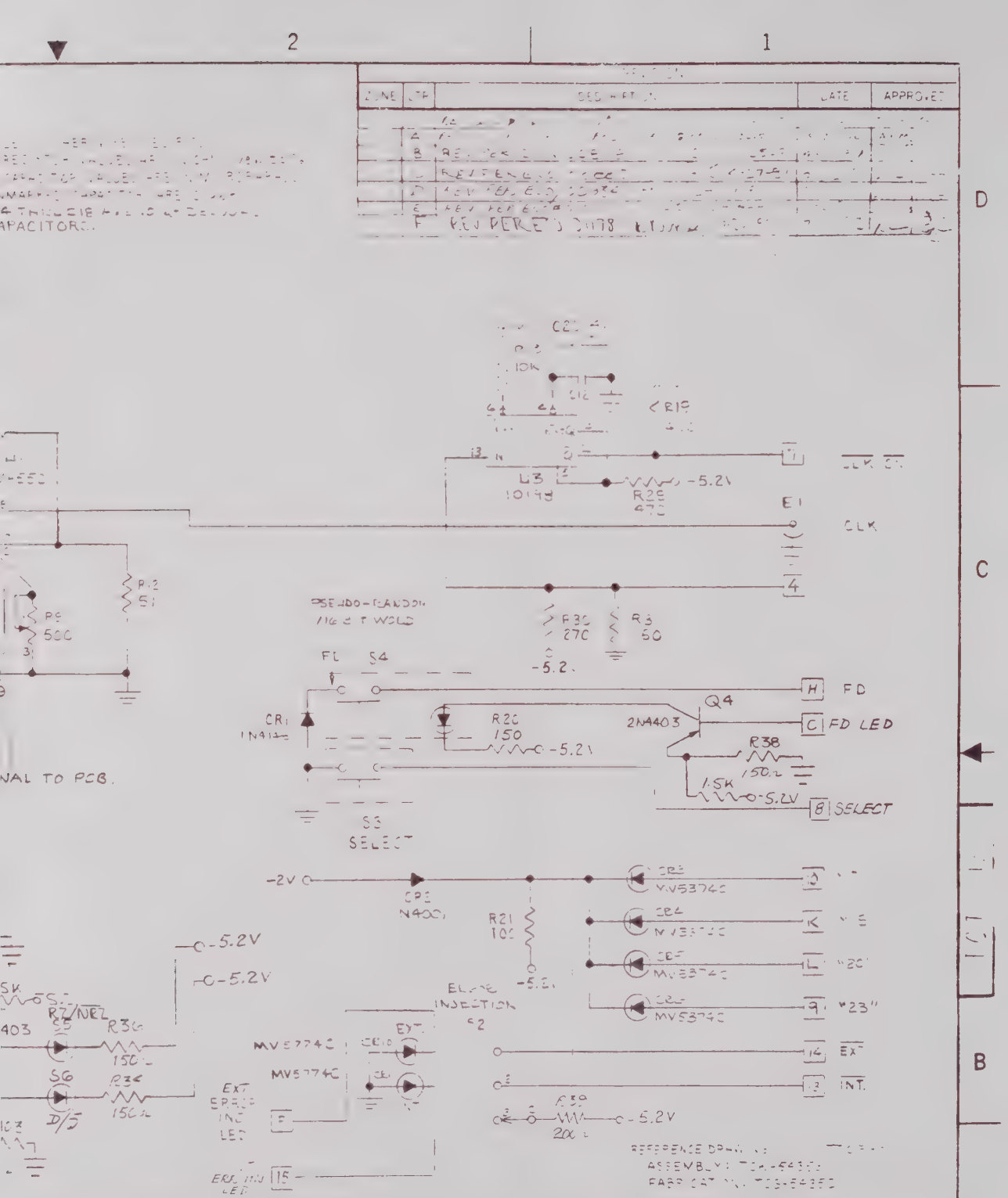


FIG. 8-B
1 of 1

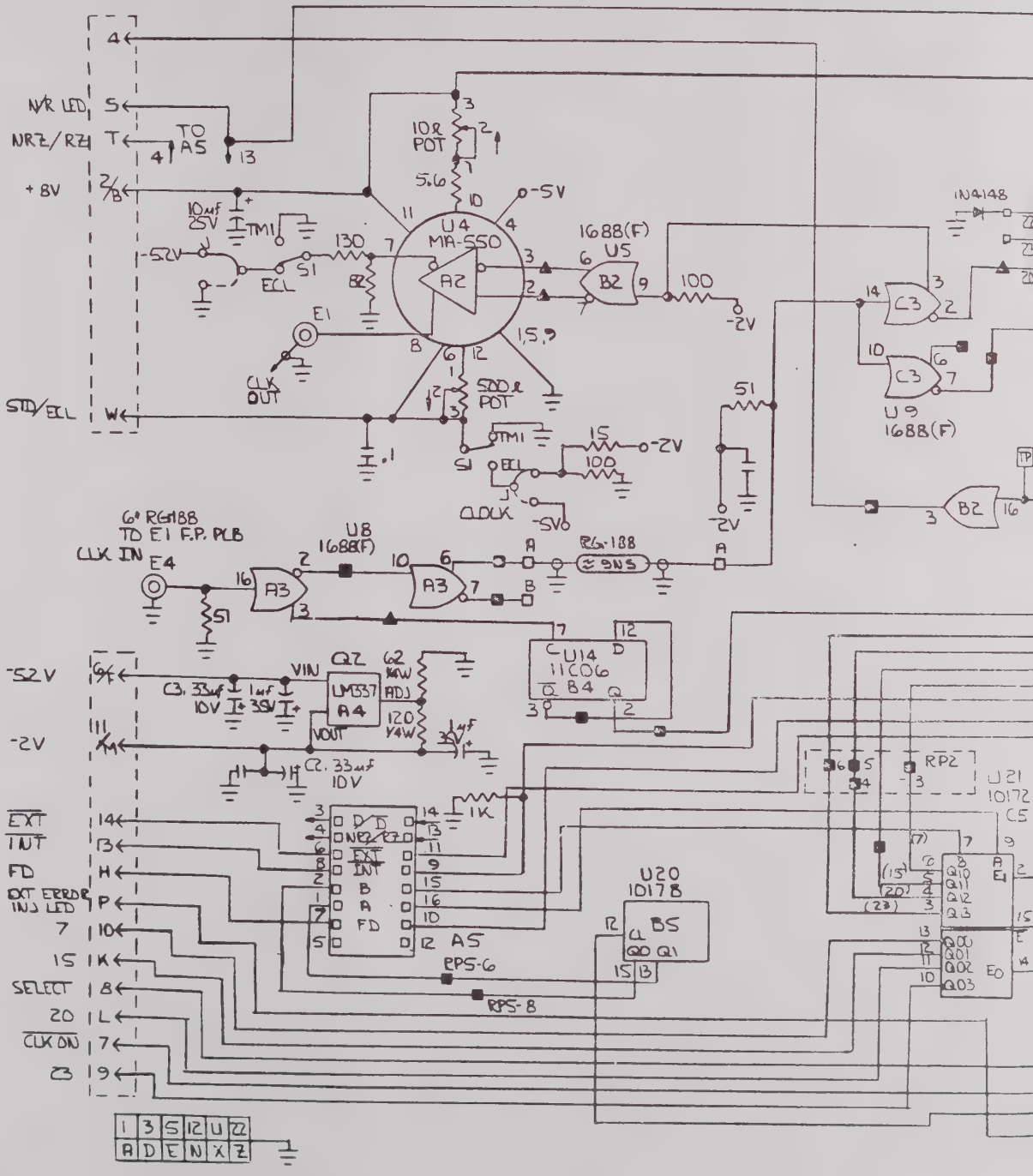
MN-302
SYSTEM BLOCK
DIAGRAM


CLK IN
J1
S1
INP
C19
4.7
R6
5 1/4K
-2V
-5.2V
E2
+8V
E3 +5V
R7
47
C7
C8
R28
10
DATA INH. IN
J2
EXT. ERROR
J3
SYNC OUT
J4
MAIN DATA
DELAYED DATA
MAIN DATA
D'L'D DATA
CLK
TMI/ECL
NRZ/RZ
D/D̄
Q1 2N4403
Q2 2N4403
Q3 2N4403
R22 1K
R23, 1K
R24, 1K
R14 200
R13, 200
R32 300
R33 200Ω
R37 150Ω
C13
C28
S5 RZ/NRZ
N/R LED
D/D LED
Q6 2N4
1.5K
-5.2V
E4
WHERE APPLICABLE
REMOVE ALL BURRS & BR
SHARP EDGES TO 1/64
TCR-5Y353
NEXT ASSY
USED
APPLICATION



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO	tau-tron inc	
TOLERANCES: ANGLES ±	DR		
FRACTIONS ±	CHK	DRAWING TITLE	
3 PLACE DECIMALS ±	APPD	MN 302	
2 PLACE DECIMALS ±		FRONT PANEL SCHEMATIC	
1 PLACE DECIMALS ±			
MATERIAL:	APPROVED	SIZE / CODE IDENT NO. / DRAWING NO.	REV F
	BY DIRECTION OF	SCALE	SHEET

Fig. 8-9
1 of 1

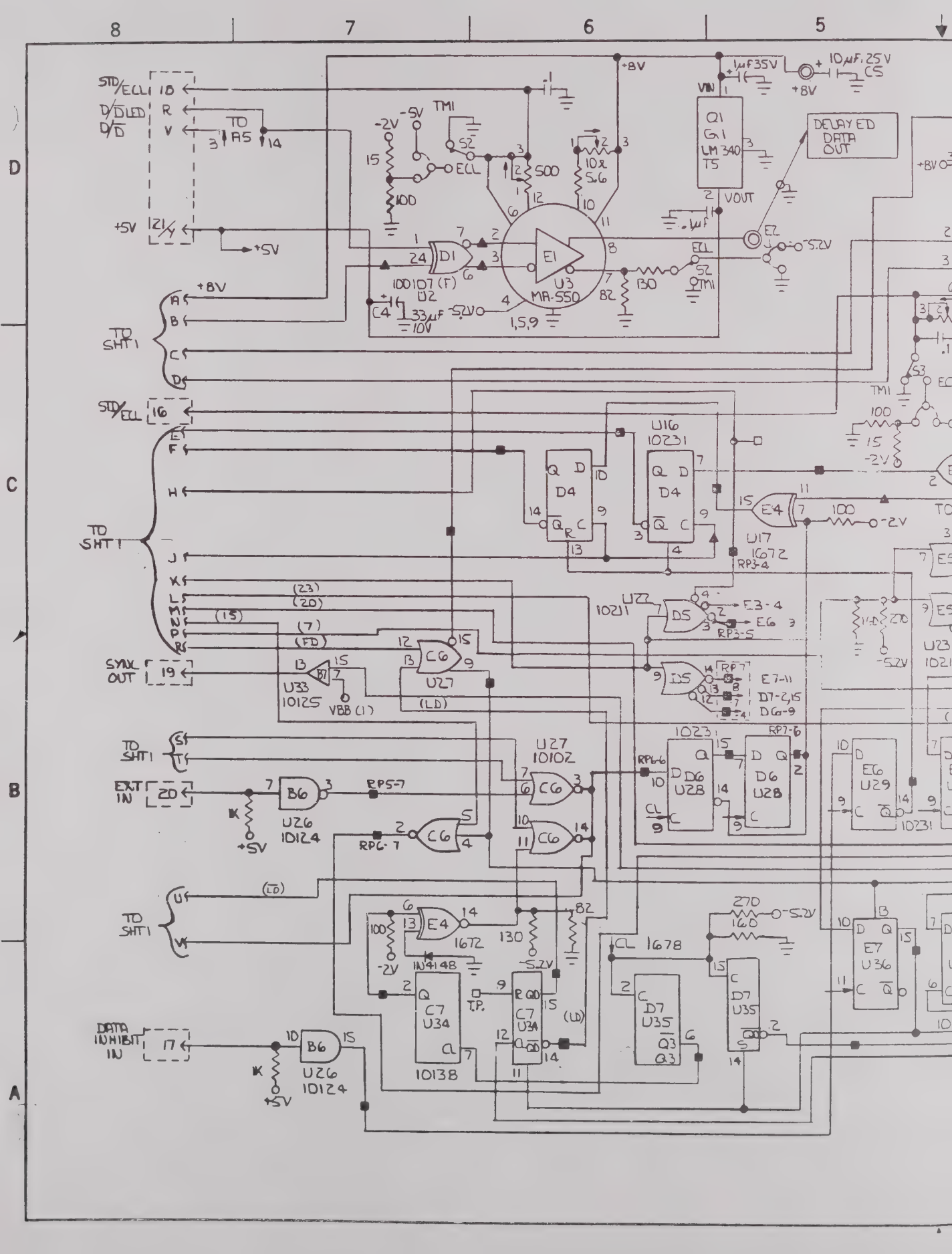


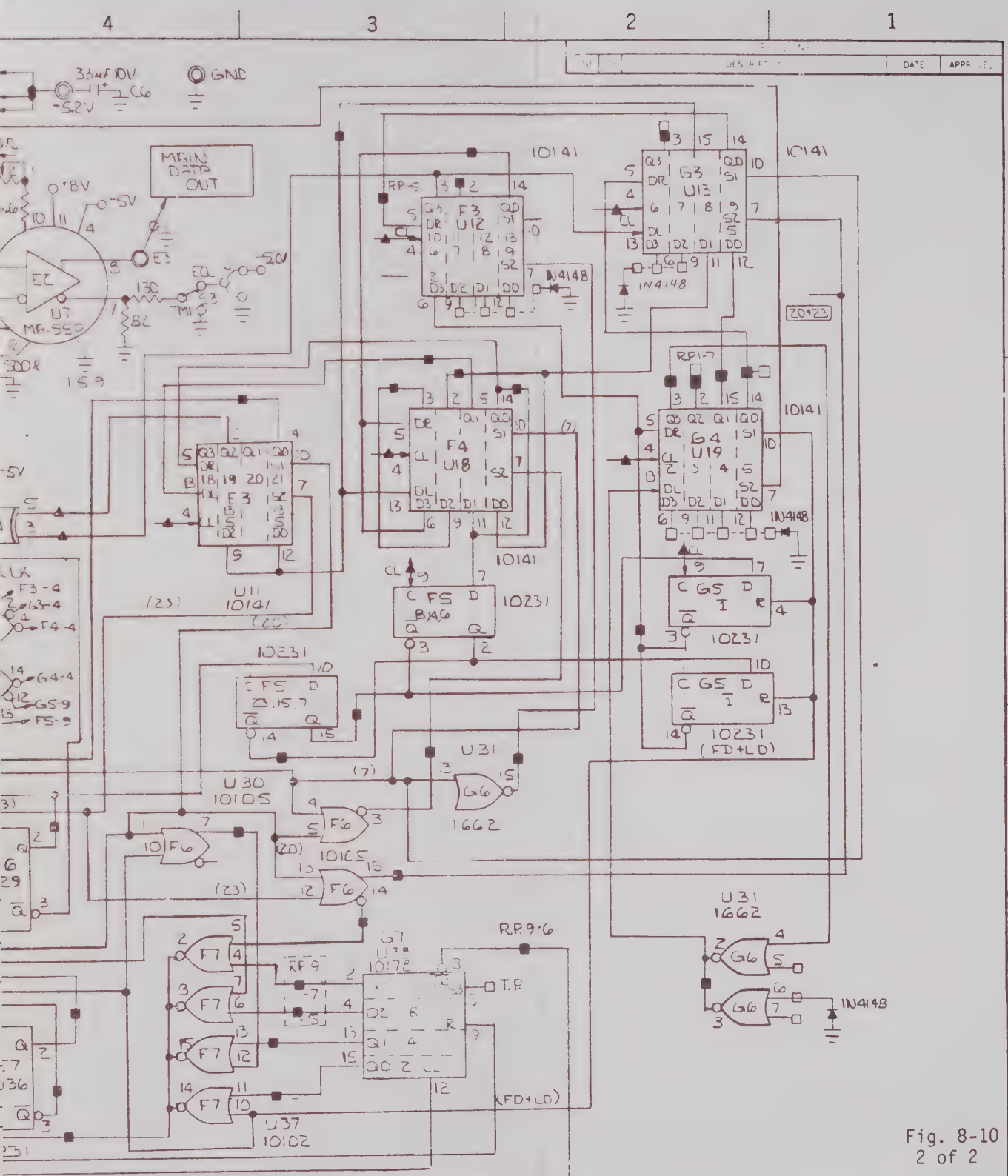
NOTES:

UNLESS OTHERWISE SPECIFIED

1. A; RESISTOR VALUE ARE IN OHMS ±5%.
   B CAPACITOR VALUE ARE MICROFARADS.
2. DENOTE:
   A. ▲ 100Ω TO -2V
   B. ● 470Ω TO -5.2V
   C. □ PAD OR TEST POINT

4
3
2
1
D
C
B
A
E REDRAWN PER ECO 01095 4-14-82
U1
100141(F)
C1
U6
1688(F)
U10
11C06
D3
D2
D1
1K
100
+5V
-2V
C4
U15
100102(F)
+8V
A
B
C
D
E
F
H
J
K
L
M
N
P
R
TO SHT 2
(23)
(20)
(15)
(7)
INT ERROR INJ LED
FD LED
S
T
U
V
TO SHT 2
1N414B
100K
10M
10K
A7
10124
U26
D1
100107(F)
BG
RPS-S
A7
U33
10125
B7
VBB(1)
VBB(1)
Fig. 8-10
1 of 2
D-54354
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL
NEXT ASSY
USED ON
APPLICATION
CONTR NO
DR
CHK
APPROVED
BY DIRECTION OF
4-14-82
5-4-82
5-4-82
tau-tron inc
DRAWING TITLE
CODE GENERATOR PCB SCHEMATIC
SIZE
D
CODE IDENT NO
DRAWING NO
D-54354
REV
E
SCALE
MN-302
SHEET 1 OF 2

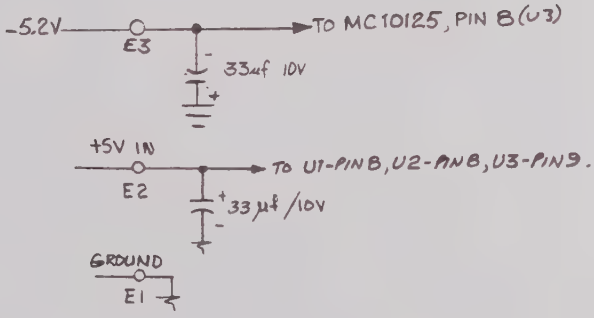

8
7
6
5
D
C
B
A
STD/ECL
D/D LED
D/D
TO A5
+5V
+8V
-5V
-2V
TM1
S2
ECL
500
100
10 & 5.6
Q1 G1 LM 340 T5
VIN
VOUT
1µF 35V
10µF, 25V
CS
DELAY ED DATA OUT
.1µF
E2
-5.2V
D1
E1
U3 MA-550
100107 (F) U2
C4 33µF 10V
1,5,9
82
130
TO SHT 1
S3
100
15
U116 10231
D4
E4
U17 1672
RP3-4
U22 10231
D5
E3-4
E6
RP3-5
SYNC OUT
U33 10125
VBB (1)
C6
U27
(LD)
U27 10102
RP7
E7-11
D7-2,15
D6-9
RP7-6
D6 U28
E6 U29
EXT IN
B6
U26 10124
RP5-7
RP6-7
1K
270
160
1N4148
T.P.
C7 U34
10138
CL
1678
D7 U35
Q3
E7 U36
DATA INHIBIT IN


4
3
2
1
D
C
B
A
33uF 10V
GND
-5.2V
MAIN DATA OUT
+8V
-5V
-5.2V
E2
U7
MC-550
130
82
TP1
E3
ECL
500R
159
10141
RP-5
F3
U12
IN4148
G3
U13
RP1-7
F4
U18
G4
U19
U11
10141
(23)
(20)
CL
FS
B/A6
10231
G5
(FD+LD)
U31
1662
G6
U30
10105
F6
(7)
RP9-6
G7
U38
10178
RP9
T.R
F7
U37
10102
(FD+LD)
D-54354
Fig. 8-10
2 of 2
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL
NEXT ASSY
USED ON
APPLICATION
CONTR NO
DR
CHK
APPD
APPROVED
BY DIRECTION OF
tau-tron mc
DRAWING TITLE
CODE GENERATOR SCHEMATIC
SIZE D
CODE IDENT NO
DRAWING NO D-54354
REV E
SCALE
MN-302
SHEET 2 OF 2

4 3

D C B A

16 PIN FLAT RIBBON CABLE FROM CODE GENERATOR BOARD LOCATION A5 (MN-302)



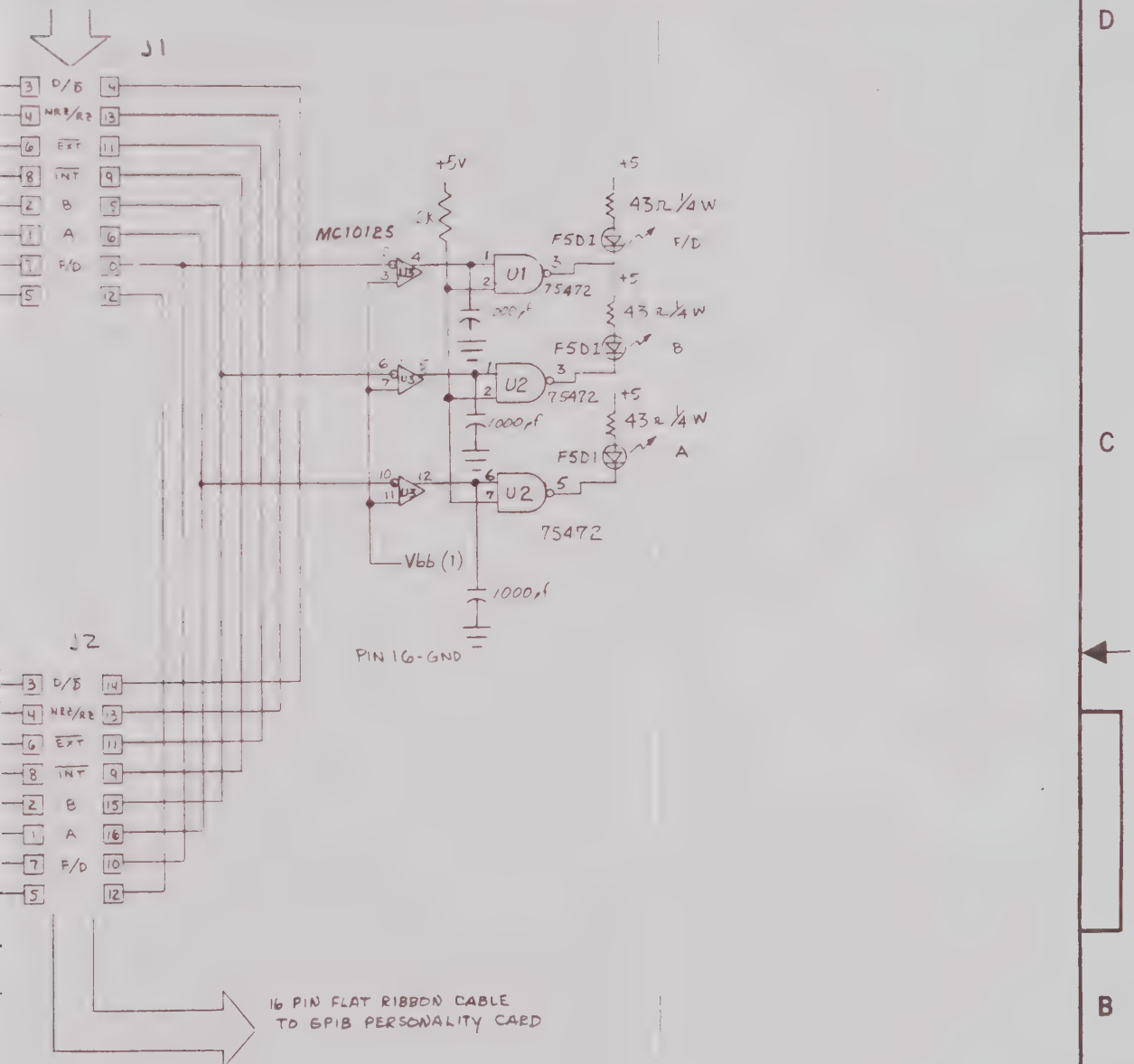
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTOR VALUES ARE IN OHMS, ¼W, ±5%.
   B. CAPACITOR VALUES ARE IN MICROFARADS.

WHERE APPLICABLE
REMOVE ALL BURRS & BRE
SHARP EDGES TO 1/64

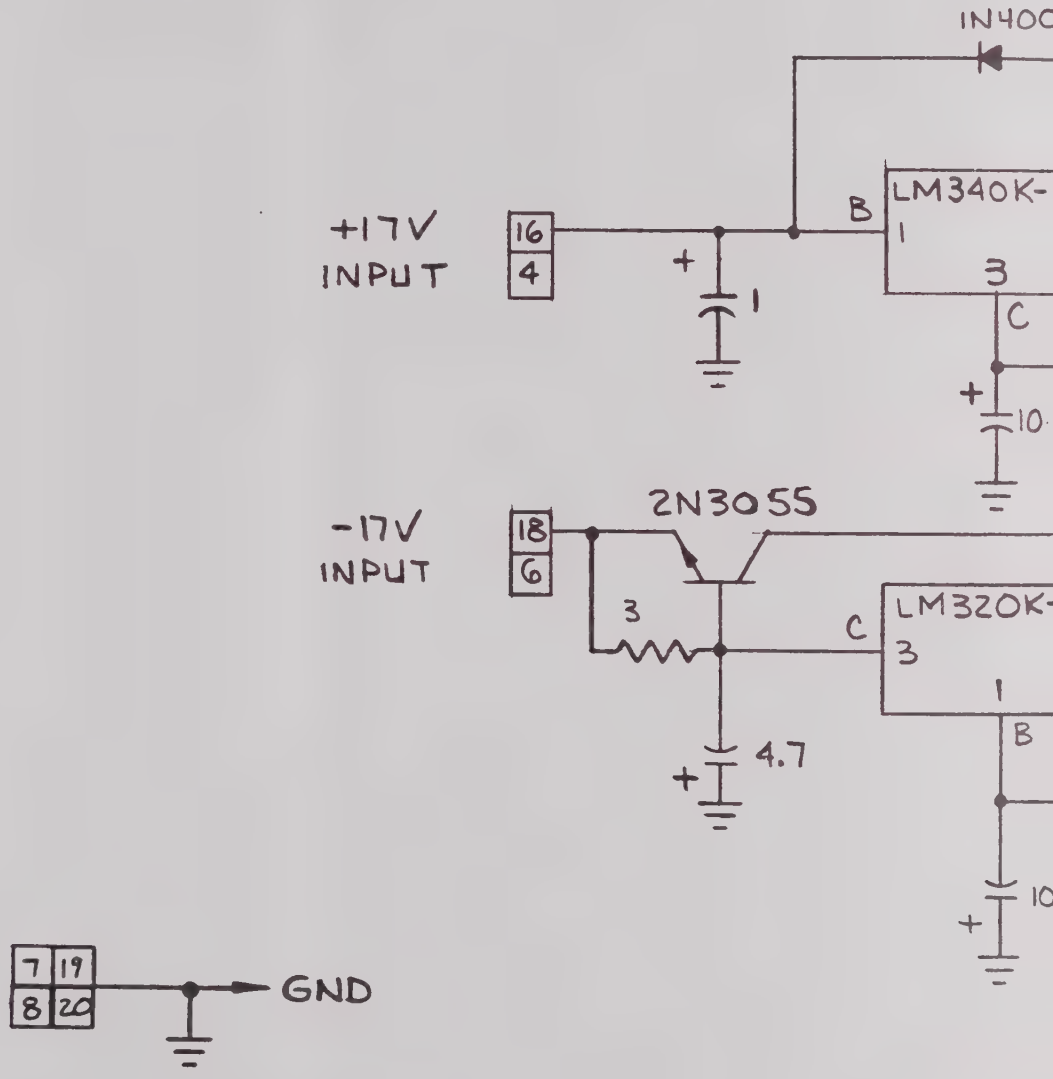
TCK-59454	MN-302
NEXT ASSY	USED O
APPLICATION	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	CHANGED PER ECO/COPY	4-?	
	A	REL PER ECO# 09-< 27	7-9-81	



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:	CONTR NO.	tau-tron inc	
	DR DEGRADEN 10/23/80 CHK B. Cooper 1-6-81 APPD PR/Vandam 2-17-81	DRAWING TITLE MN-302 OPTICAL INTERFACE BOARD	
	APPROVED BY DIRECTION OF	SIZE C · CODE IDENT NO. · DRAWING NO. TCJ-54452 · REV A SCALE — · MN-302 · SHEET 1 OF 1	

Fig. 8-11
1 of 1



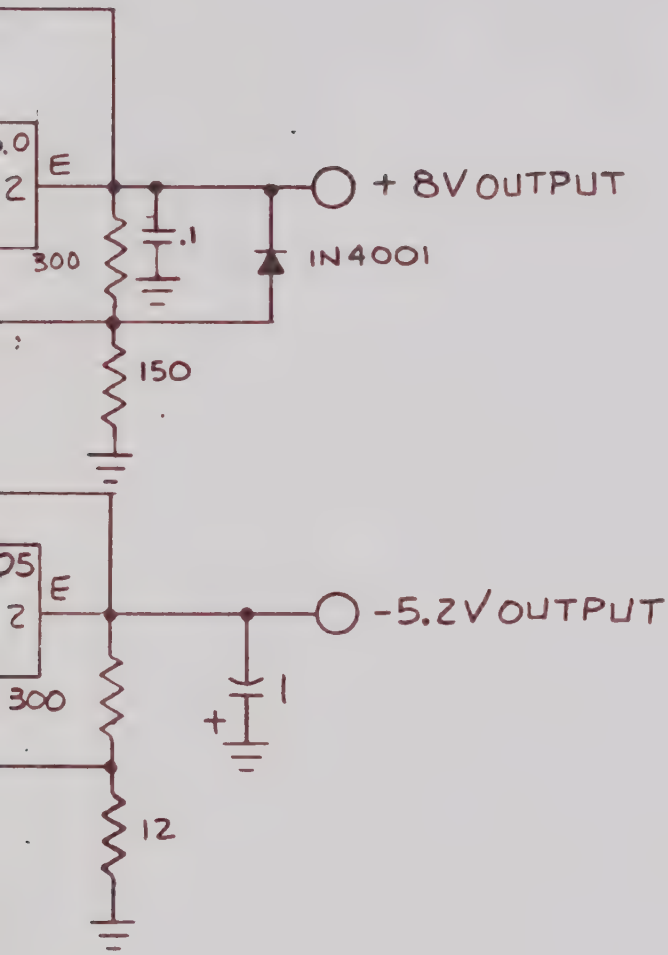
NOTES:

1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
   b) CAPACITANCE VALUES ARE IN MICRO FARADS.
2. ☐ INDICATES 24 PIN POWER CONNECTOR

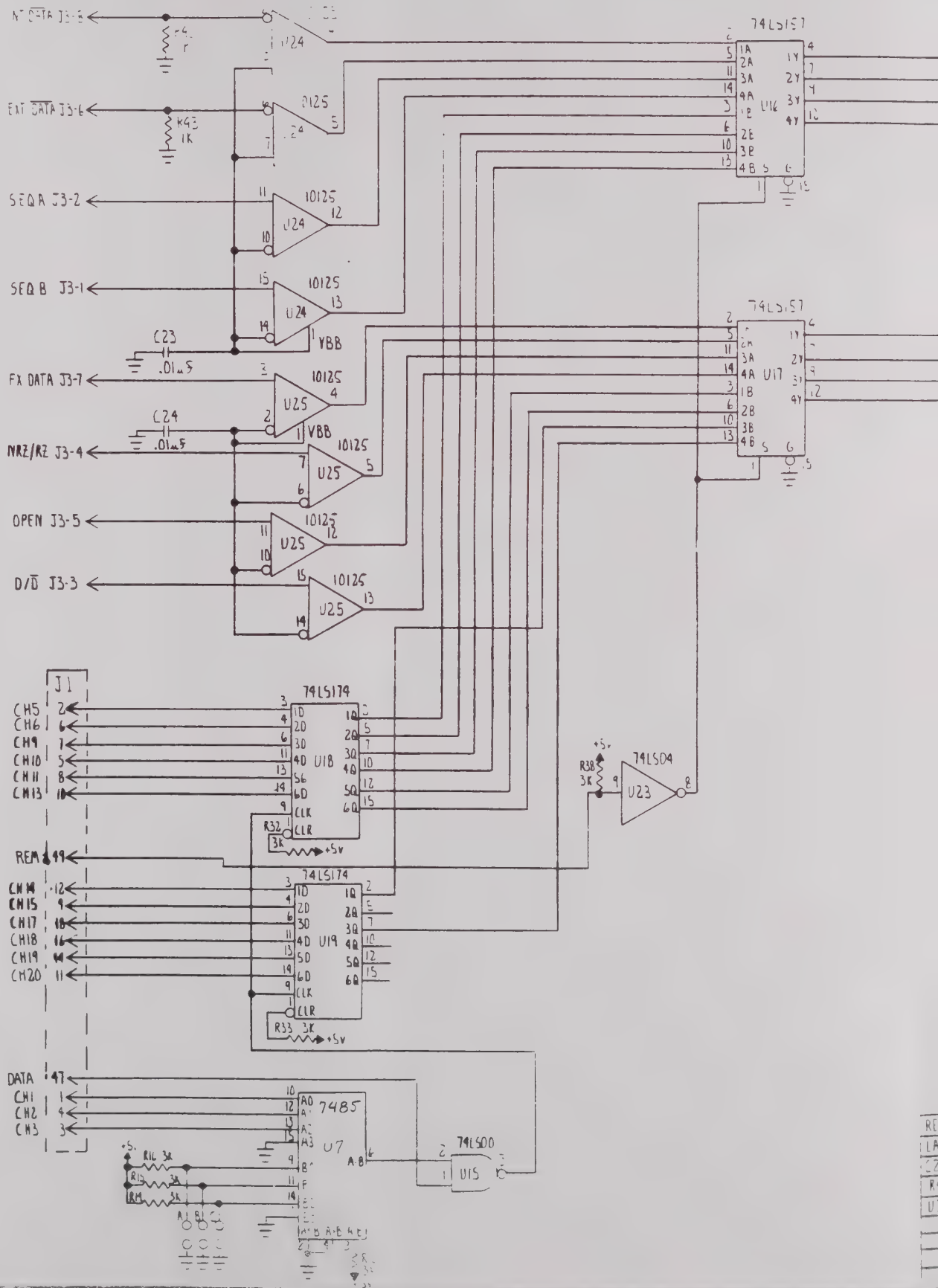
WHERE APPLICABLE: REMOVE ALL BURRS & BREA SHARP EDGES TO 1/64.	
TEK-54408	MN-302
NEXT ASSY	USED ON
APPLICATION	

3	2	1

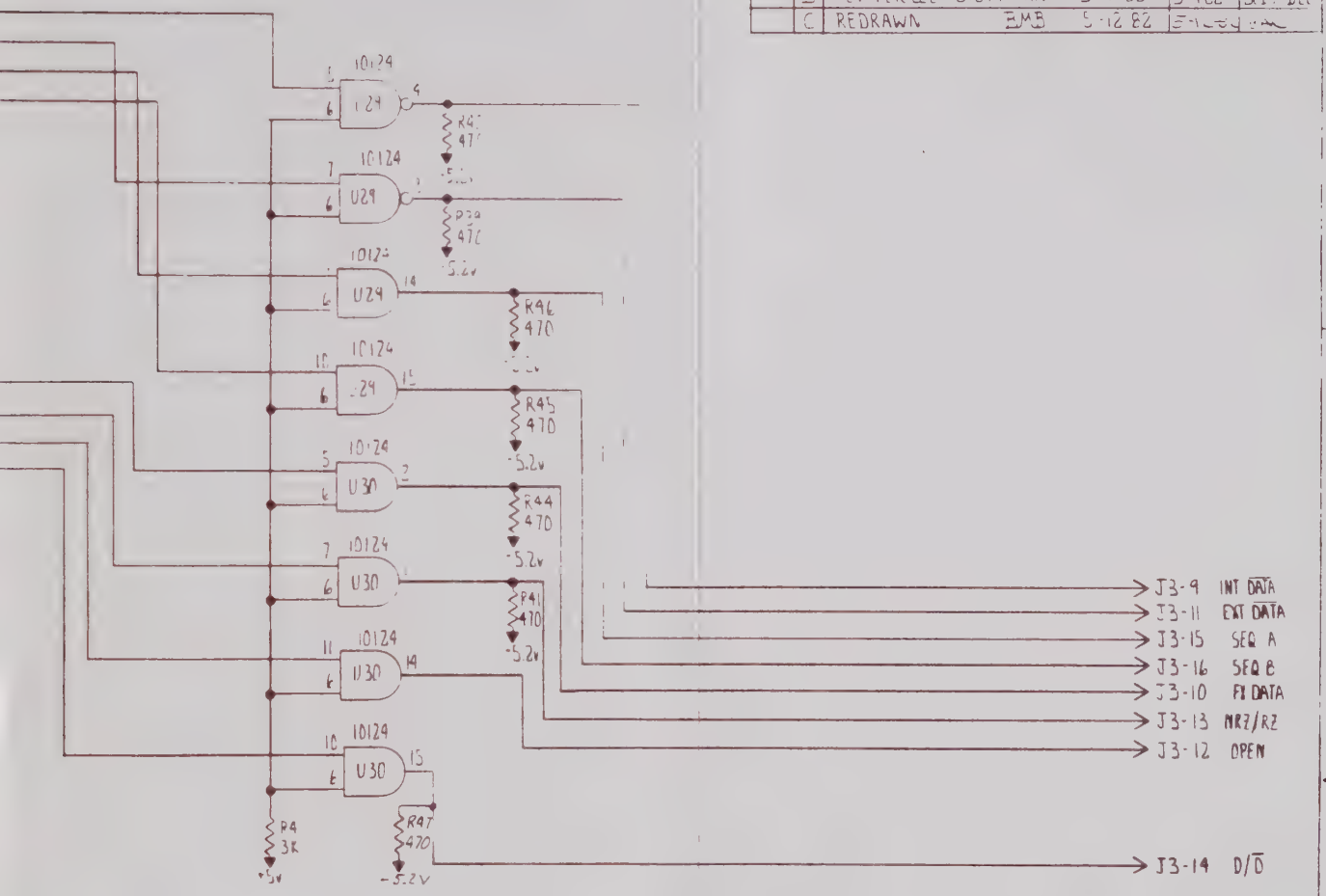
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

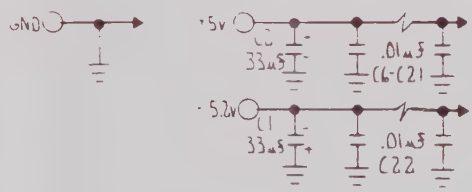


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± — FRACTIONS ± — 3 PLACE DECIMALS ± — 2 PLACE DECIMALS ± — 1 PLACE DECIMALS ± —	CONTR NO.	tau-tron inc	Fig. 8-12 1 of 1
MATERIAL: —	DR M. Castello 13May80 CHK [illegible] 13May80 APPD	DRAWING TITLE POWER SUPPLY SCHEMATIC (+8V) - 5V BOOST	
	APPROVED BY DIRECTION OF	SIZE B / CODE IDENT NO. / DRAWING NO. TBJ - 54407 / REV O SCALE — / TM1 SERIES / SHEET 1 OF 1	


EXT DATA J3-6
SEQ A J3-2
SEQ B J3-1
FX DATA J3-7
NRZ/RZ J3-4
OPEN J3-5
D/D̄ J3-3
10125
U24
U25
C23
C24
.01uF
VBB
74LS157
U16
U17
74LS174
U18
U19
74LS04
U23
74LS00
U15
7485
U7
J1
CH5
CH6
CH9
CH10
CH11
CH13
CH14
CH15
CH17
CH18
CH19
CH20
REM
DATA
CH1
CH2
CH3
R32
R33
R38
3K
+5V

		REV PER ECO #C0013	JRT	17 JUN 81	
	B	REV PER ECO #01077	RN	3-4-82	
	C	REDRAWN	EMB	5-12-82	





NOTES
1. UNLESS OTHERWISE SPECIFIED.
   A) RESISTANCE VALUES ARE IN OHMS' 1/8W ±5%
   B) CAPACITANCE VALUES ARE IN MICROFARADS

Fig. 8-13
1 of 1

ERENCE DESIGNATIONS	
T USED	UNUSED
	R13

WHERE APPLICABLE
REMOVE ALL BURRS & BREAK
SHARP EDGES TO 1/64

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

DRAWN	C PERLMUTTER	2/9/82
CHK'D	C COOPER	4/19/82
APPROVED	C PERLMUTTER	5/17/82

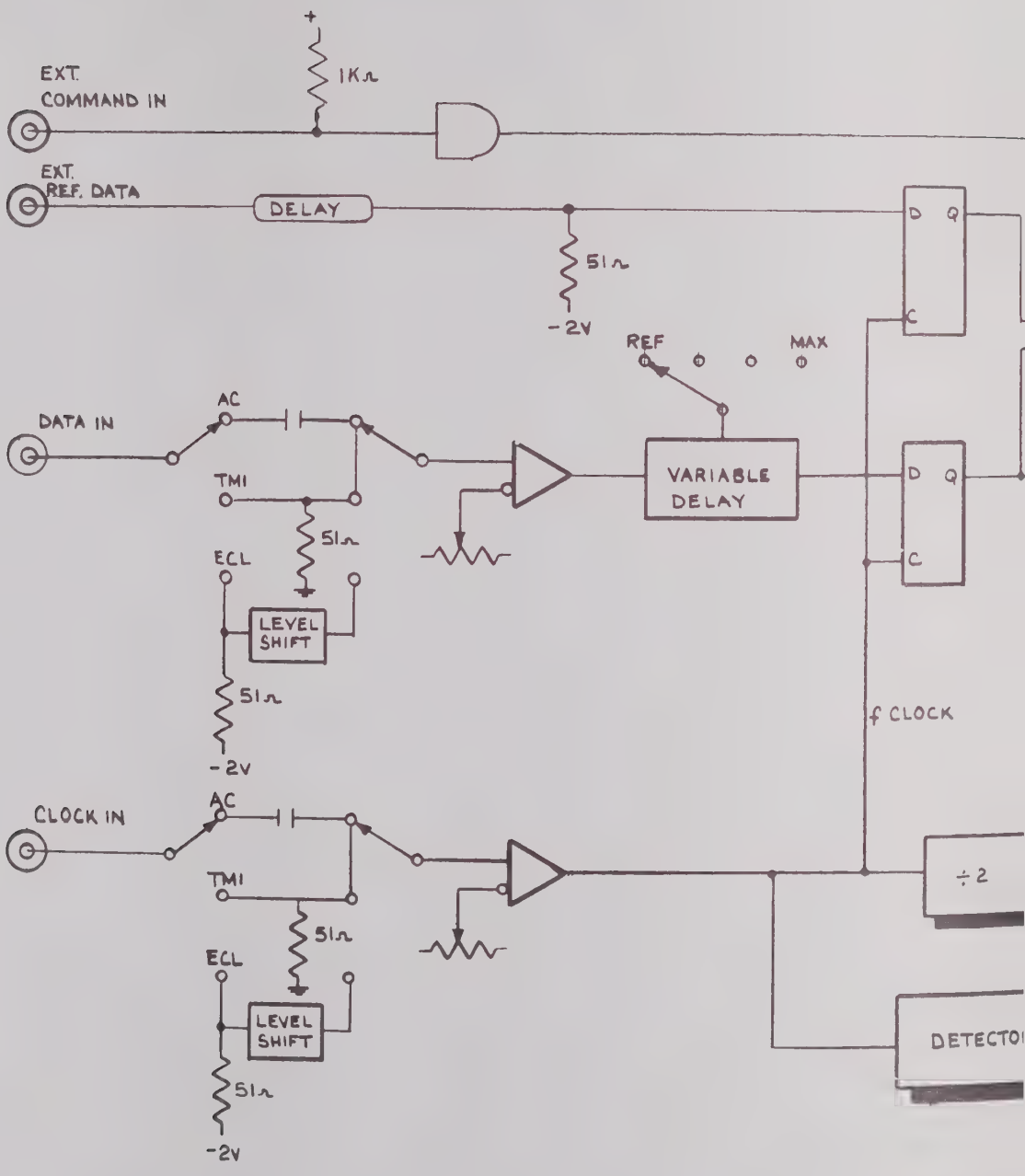
tau-tron

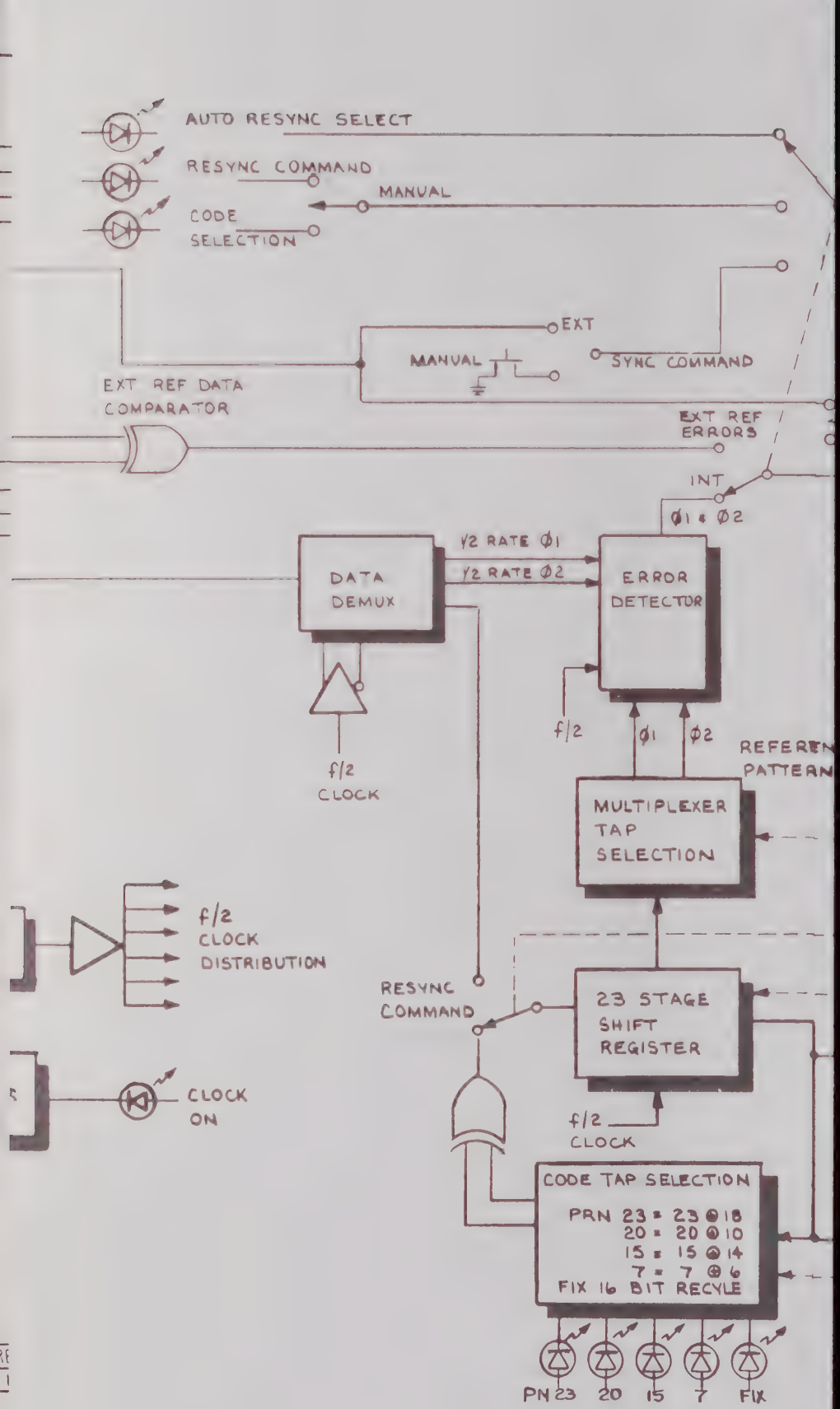
SCHEMATIC
MN-302
TM1 MODULE GPIB ADAPTOR

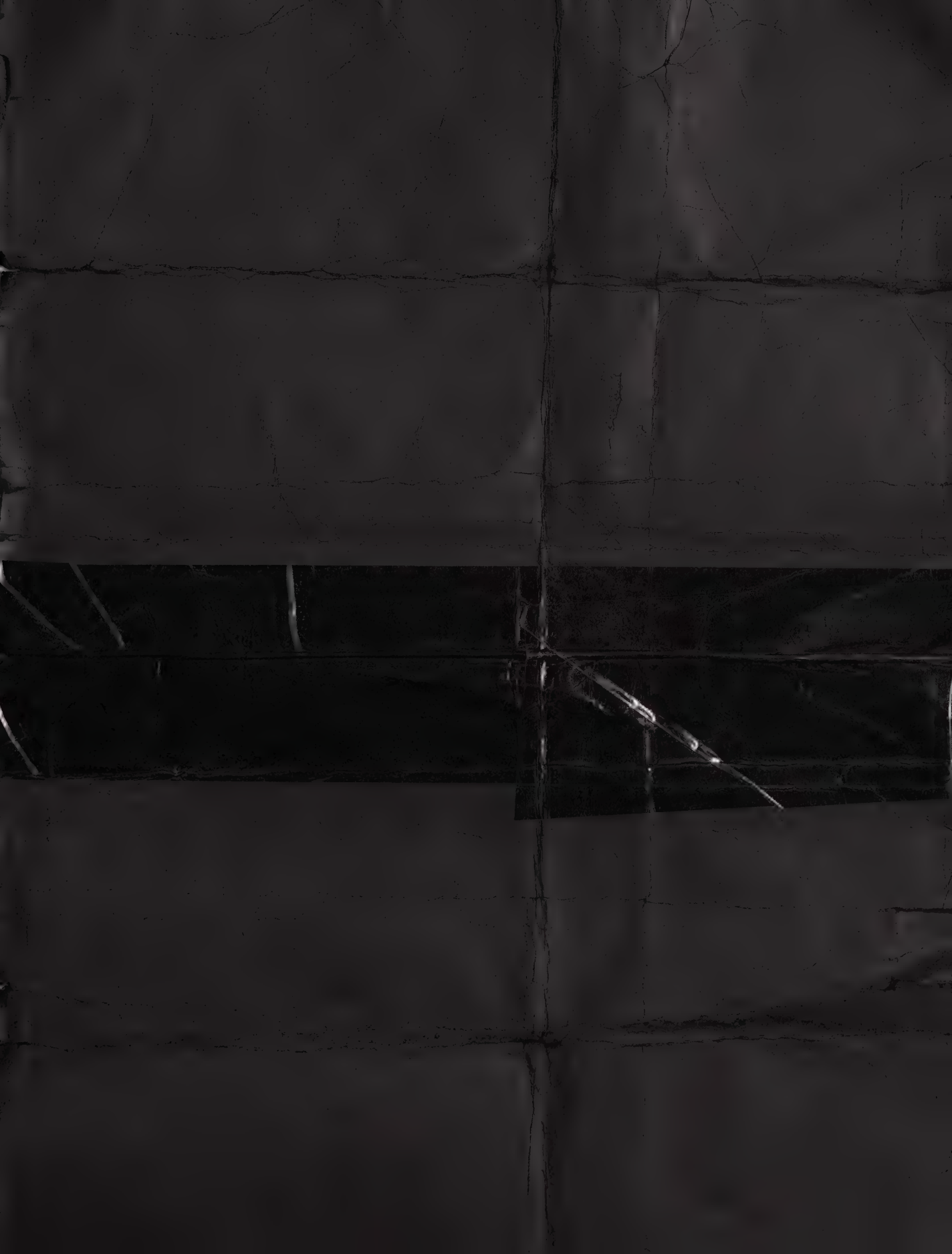
D-54539	MN-302
NEXT ASSY	USED ON
APPLICATION	

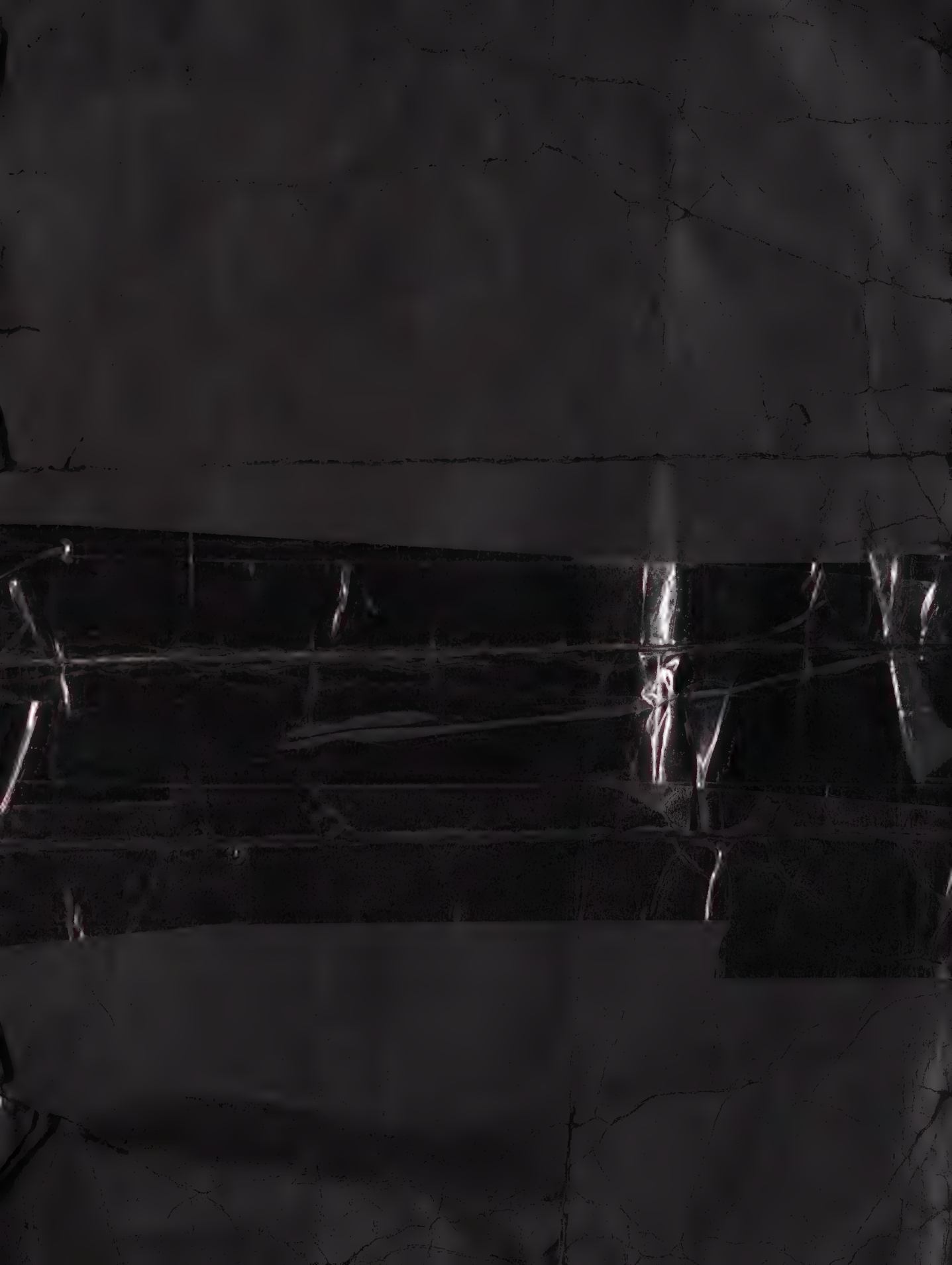
SIZE	CODE IDENT NO	DRAWING NO	REV
D		D-54538	C
SCALE	TM1 CHIC	SHEET 1 OF 1	

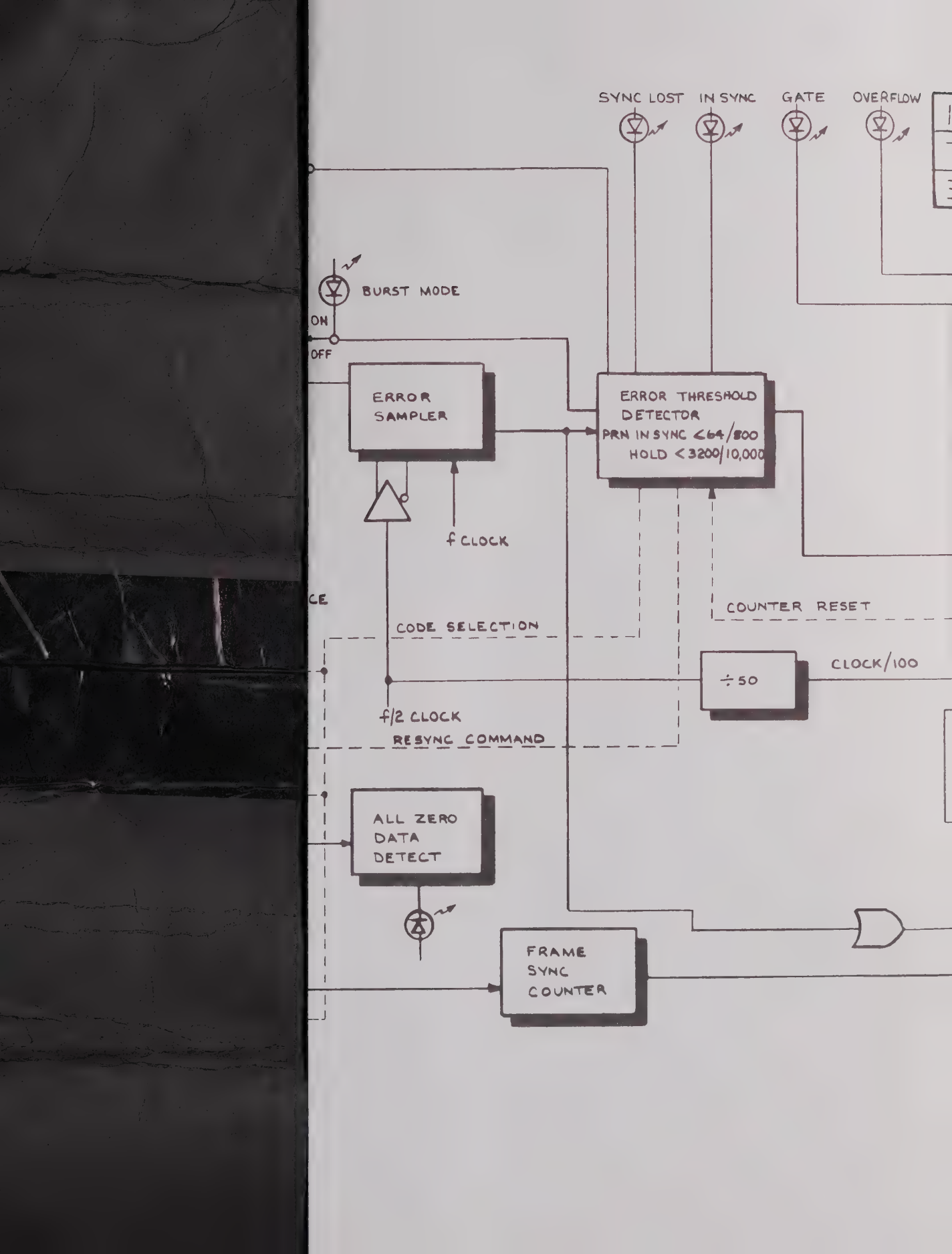
D-54538


EXT.
COMMAND IN
+
1K Ω
EXT.
REF. DATA
DELAY
51 Ω
-2V
D Q
C
REF
MAX
DATA IN
AC
TMI
51 Ω
ECL
LEVEL
SHIFT
51 Ω
-2V
VARIABLE
DELAY
D Q
C
f CLOCK
CLOCK IN
AC
TMI
51 Ω
ECL
LEVEL
SHIFT
51 Ω
-2V
÷2
DETECTO


AUTO RESYNC SELECT
RESYNC COMMAND
MANUAL
CODE SELECTION
EXT
MANUAL
SYNC COMMAND
EXT REF DATA COMPARATOR
EXT REF ERRORS
INT
Ø1 & Ø2
DATA DEMUX
½ RATE Ø1
½ RATE Ø2
ERROR DETECTOR
f/2 CLOCK
f/2
Ø1
Ø2
REFEREN PATTERN
MULTIPLEXER TAP SELECTION
f/2 CLOCK DISTRIBUTION
RESYNC COMMAND
23 STAGE SHIFT REGISTER
CLOCK ON
f/2 CLOCK
CODE TAP SELECTION
PRN 23 = 23 ⊕ 18
20 = 20 ⊕ 10
15 = 15 ⊕ 14
7 = 7 ⊕ 6
FIX 16 BIT RECYLE
PN 23
20
15
7
FIX






SYNC LOST
IN SYNC
GATE
OVERFLOW
BURST MODE
ON
OFF
ERROR SAMPLER
ERROR THRESHOLD DETECTOR
PRN IN SYNC < 64/800
HOLD < 3200/10,000
f CLOCK
CE
CODE SELECTION
COUNTER RESET
÷ 50
CLOCK/100
f/2 CLOCK
RESYNC COMMAND
ALL ZERO DATA DETECT
FRAME SYNC COUNTER

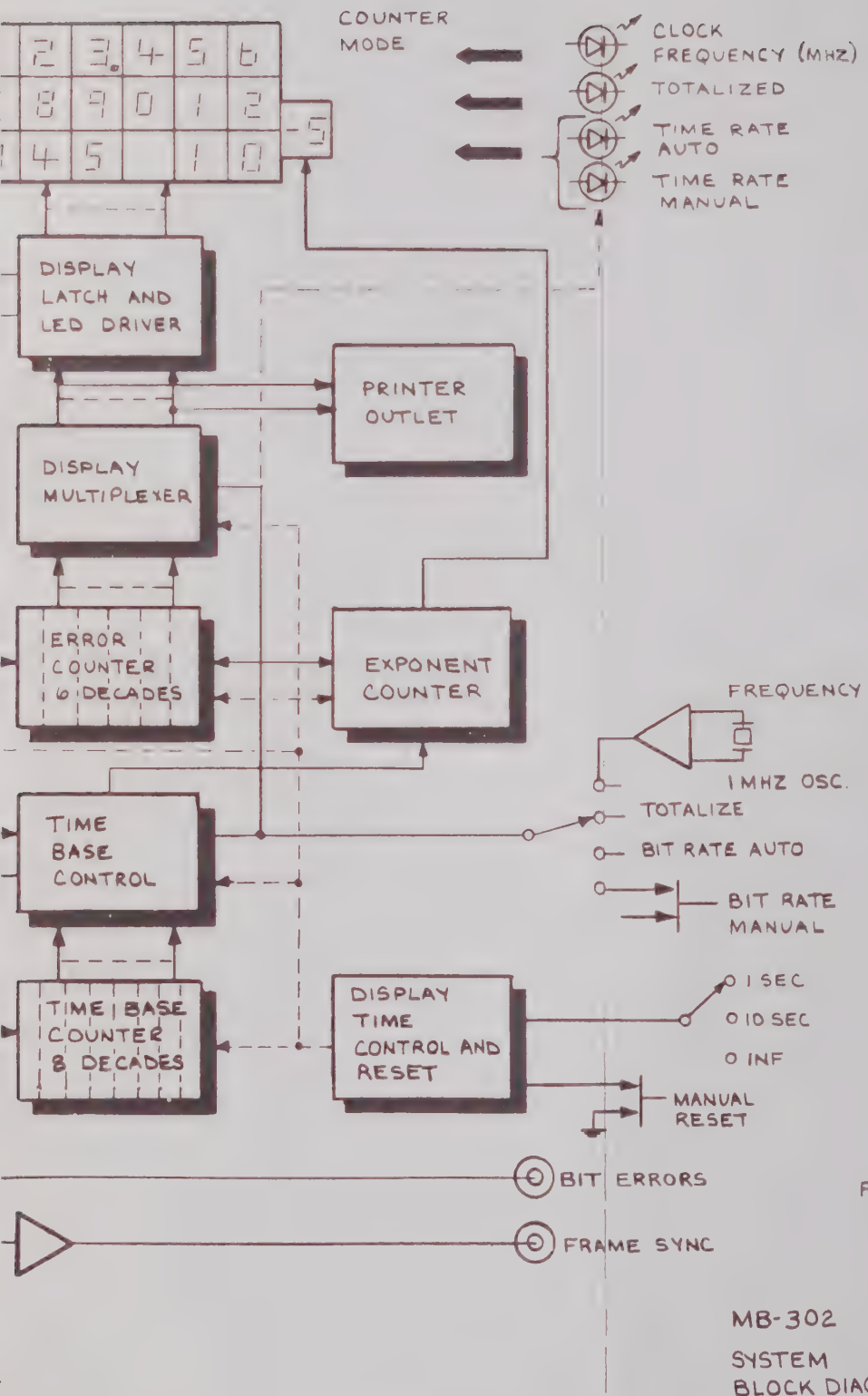


FIG. 8-14
1 of 1

MB-302
SYSTEM
BLOCK DIAGRAM

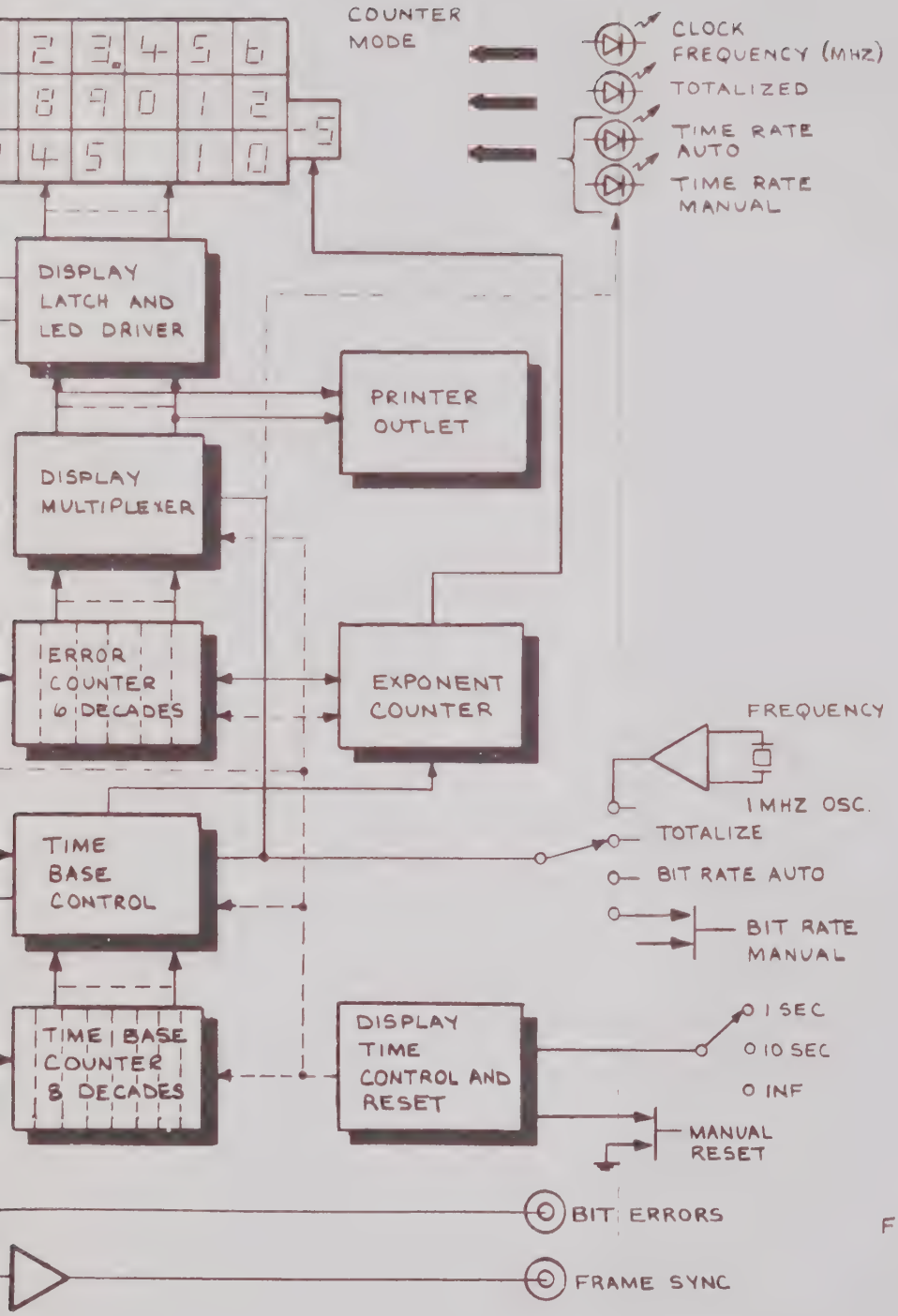


FIG. 8-14
1 of 1

MB-302
SYSTEM
BLOCK DIAGRAM

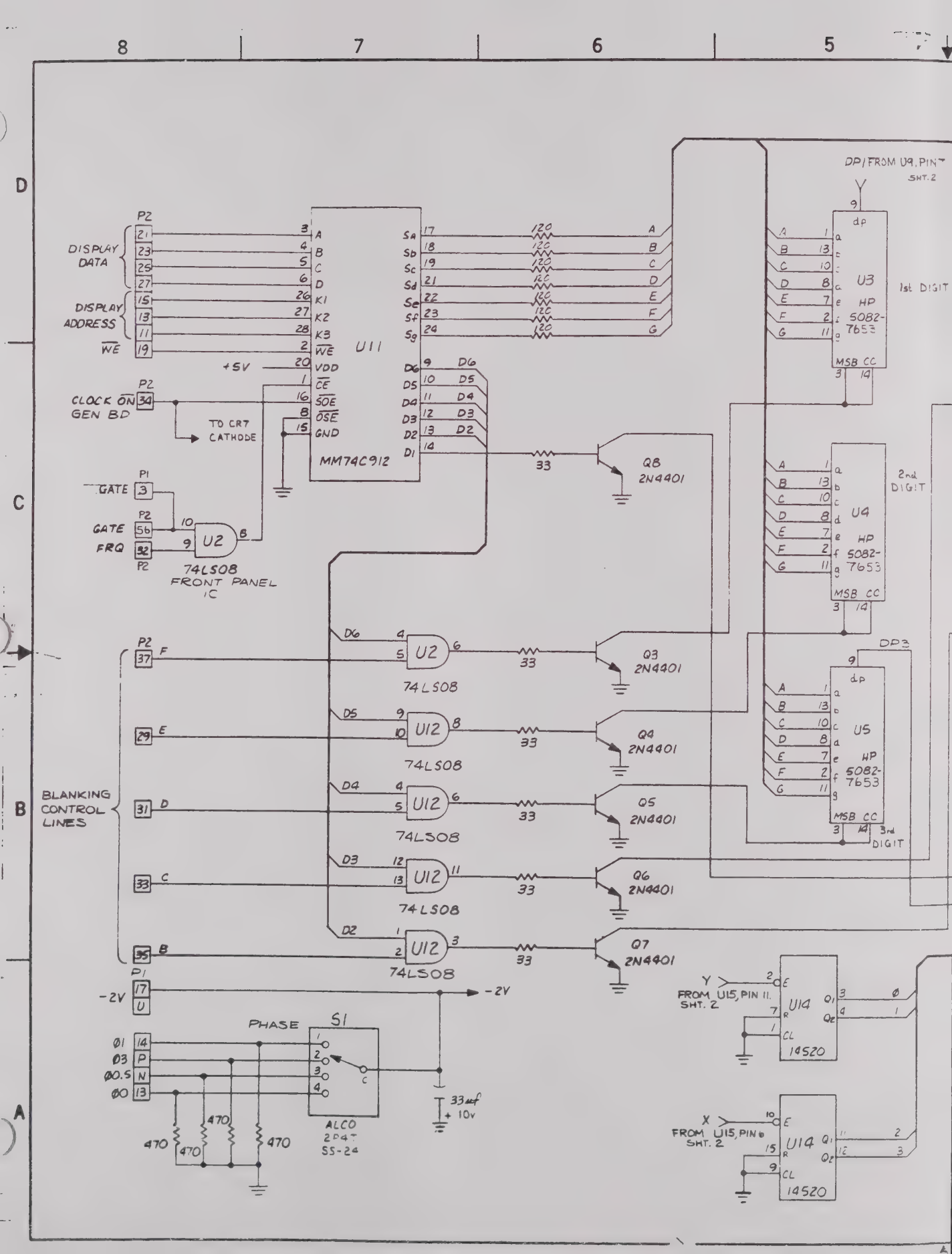

8
7
6
5
D
C
B
A
DP/ FROM U9, PIN 7 SHT. 2
DISPLAY DATA
DISPLAY ADDRESS
WE
P2
U11
MM74C912
+5V
CLOCK ON GEN BD
TO CRT CATHODE
GATE
FRQ
P1
U2
74LS08
FRONT PANEL I/C
U3
HP 5082-7653
1st DIGIT
U4
2nd DIGIT
U5
3rd DIGIT
MSB CC
DP3
Q8 2N4401
Q3 2N4401
Q4 2N4401
Q5 2N4401
Q6 2N4401
Q7 2N4401
33
BLANKING CONTROL LINES
-2V
PHASE
S1
ALCO 2P4T SS-24
470
33 uf + 10v
U14
14520
FROM U15, PIN 11. SHT. 2
FROM U15, PIN 6 SHT. 2

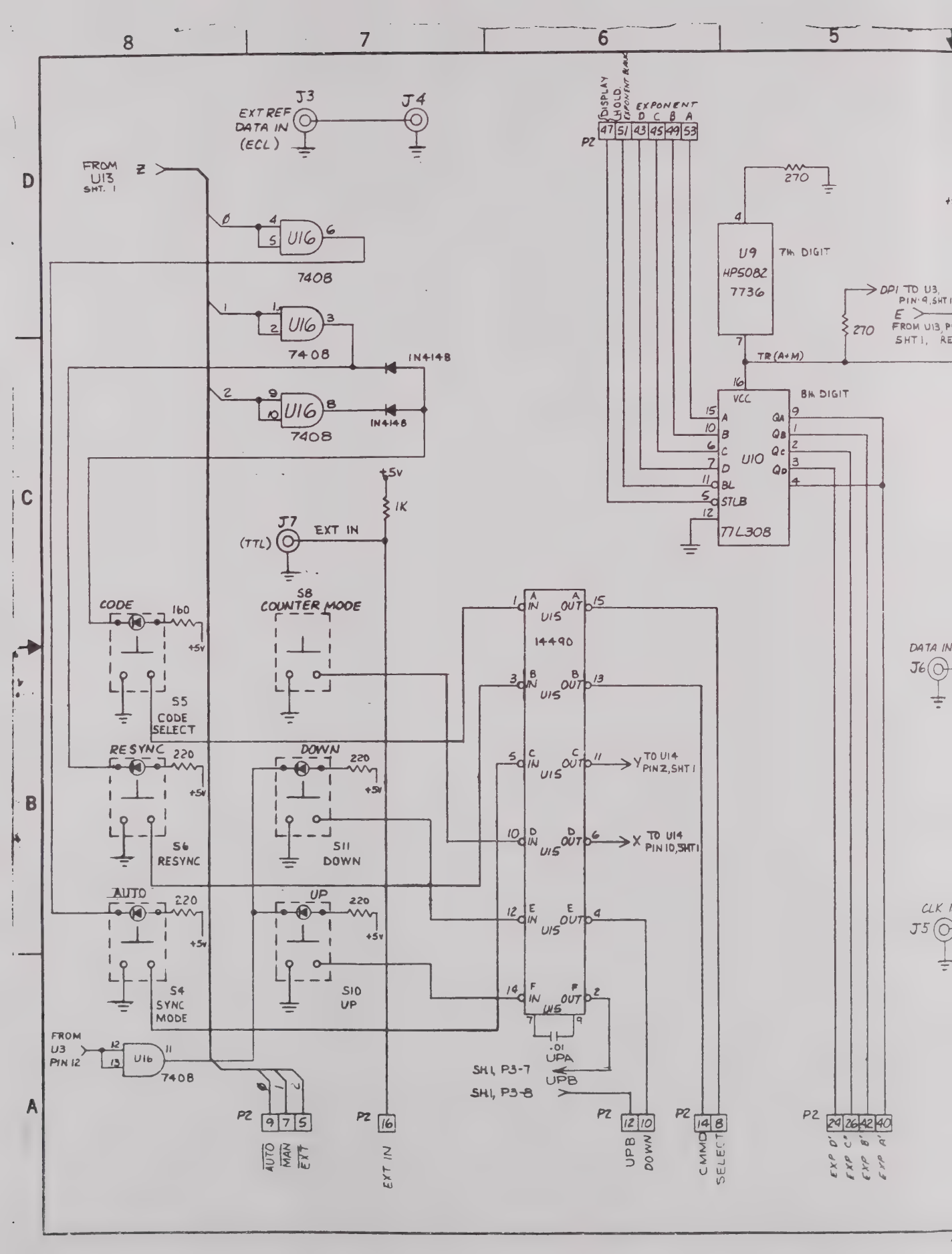
Fig. 8-15
1 of 2

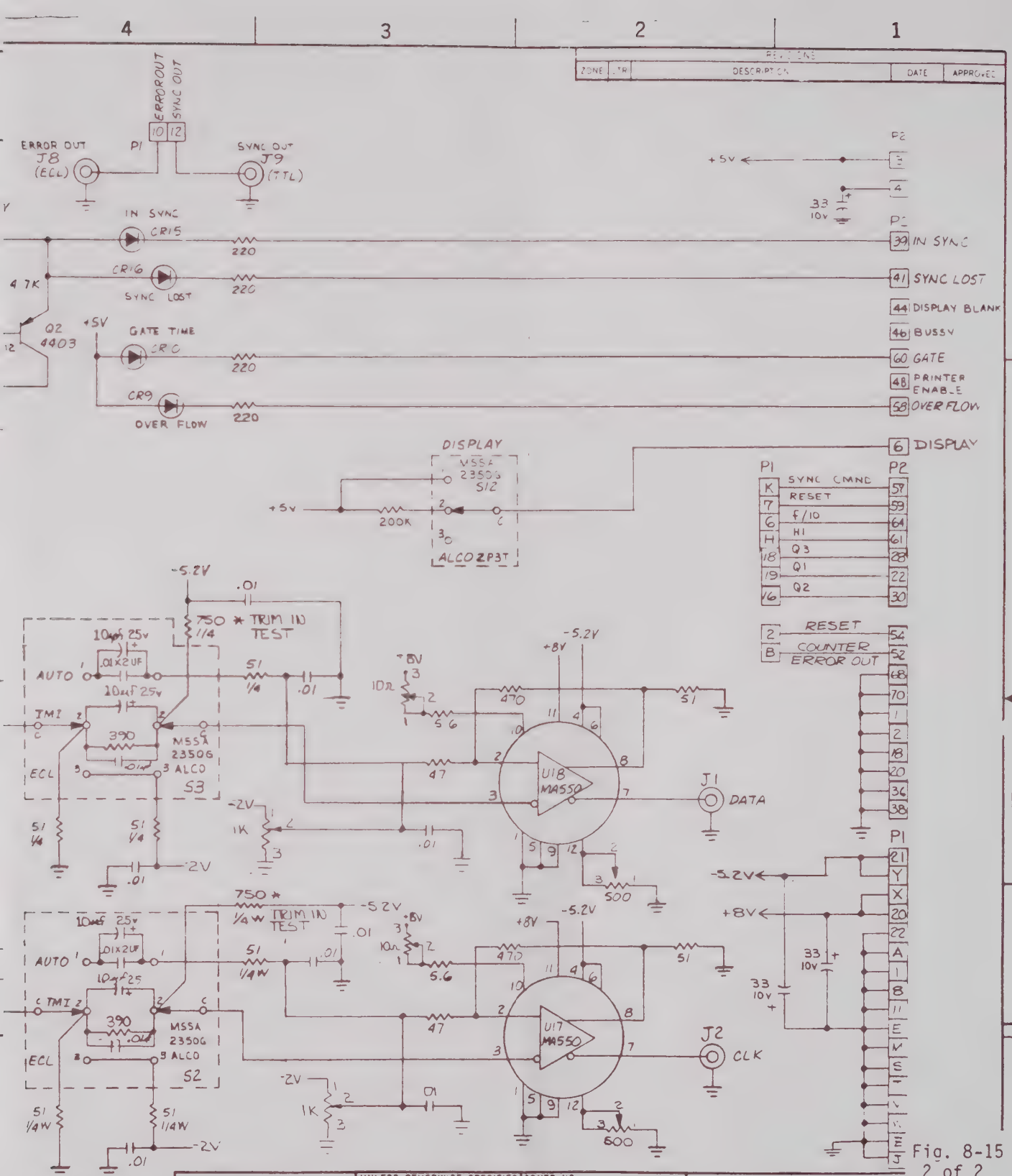
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR 12-80 CHK 11 FEB APPD 4/13/81 APPROVED BY DIRECTION OF
TDJ-54359 / MB 302 NEXT ASSY / USED ON APPLICATION		

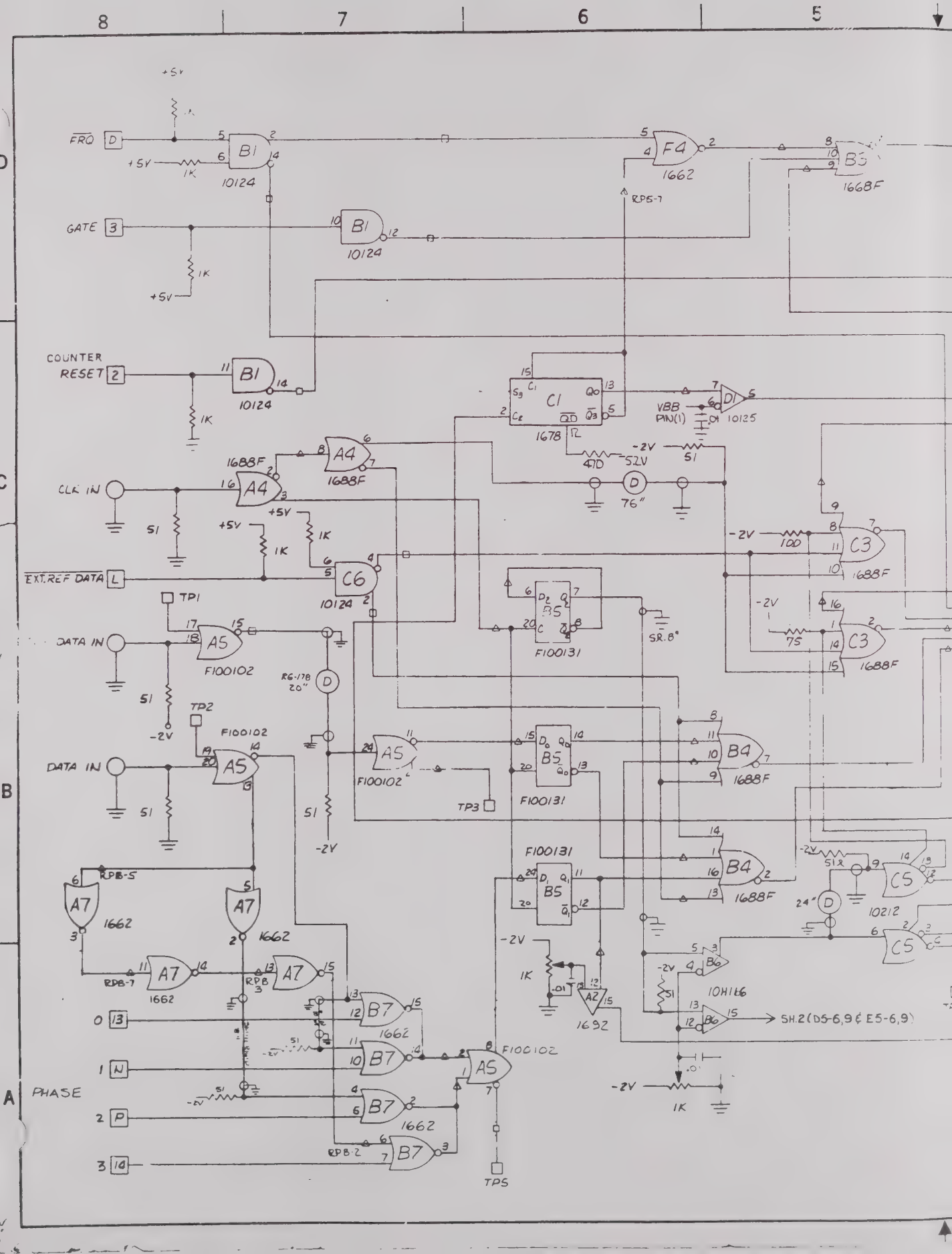
tau-tron inc

DRAWING TITLE
SCHEMATIC
FRONT PANEL PC BOARD

SIZE D | CODE IDENT NO | DRAWING NO TDJ-54357 | REV C
SCALE 2 | MB-302 | SHEET 1 OF 2


8
7
6
5
D
C
B
A
J3
EXT REF DATA IN (ECL)
J4
FROM U13 SHT. 1
Z
U16
7408
IN4148
+5V
1K
J7
(TTL)
EXT IN
S8
COUNTER MODE
CODE
160
S5
CODE SELECT
RESYNC
220
S6
RESYNC
DOWN
S11
DOWN
AUTO
S4
SYNC MODE
UP
S10
UP
FROM U3 PIN 12
P2
AUTO
MAN
EXT
EXT IN
U15
14490
TO U14 PIN 2, SHT 1
TO U14 PIN 10, SHT 1
.01
UPA
UPB
SH 1, P3-7
SH 1, P3-8
UPB DOWN
CMMD SELECT
DISPLAY HOLD
EXPONENT
D C B A
270
U9
HP5082 7736
7th DIGIT
DPI TO U3, PIN 9, SHT 1
FROM U13, P SHT 1, RE
TR (A+M)
U10
77L308
VCC
8th DIGIT
DATA IN
J6
CLK
J5
EXP D'
EXP C'
EXP B'
EXP A'


4
3
2
1
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
ERROR OUT
J8
(ECL)
P1
10
12
ERROR OUT
SYNC OUT
SYNC OUT
J9
(TTL)
P2
+5V
4
33
10V
P1
IN SYNC
CR15
220
39
IN SYNC
4.7K
CR16
SYNC LOST
220
41
SYNC LOST
44
DISPLAY BLANK
46
BUSSY
Q2
4403
+5V
GATE TIME
CR10
220
60
GATE
48
PRINTER ENABLE
CR9
OVER FLOW
220
58
OVER FLOW
DISPLAY
6
DISPLAY
MSSA
23506
S12
+5V
200K
ALCO ZP3T
P1
P2
SYNC CMND
K
57
RESET
7
59
f/10
6
64
H
61
Q3
18
28
Q1
19
22
Q2
16
30
RESET
2
54
COUNTER ERROR OUT
B
52
48
70
1
2
18
20
36
38
-5.2V
.01
750 * TRIM ID TEST
10uf 25v
.01X2 UF
AUTO
51
1/4
.01
10uf 25v
TMI
390
.01uf
MSSA
23506
ALCO
S3
ECL
51
1/4
51
1/4
-2V
.01
+8V
10K
5.6
-5.2V
+8V
470
51
47
U18
MA550
J1
DATA
-2V
1K
.01
500
P1
21
Y
X
20
22
A
1
B
11
E
M
S
-5.2V
+8V
33
10V
33
10V
750 *
1/4W
TRIM ID TEST
-5.2V
.01
10uf 25v
.01X2UF
AUTO
51
1/4W
.01
10uf 25
TMI
390
.01uf
MSSA
23506
ALCO
S2
ECL
51
1/4W
51
1/4W
-2V
.01
+8V
10K
5.6
-5.2V
+8V
470
51
47
U17
MA550
J2
CLK
-2V
1K
.01
500
J
Fig. 8-15
2 of 2
WHERE APPLICABLE
REMOVE ALL BURRS & BREAK
SHARP EDGES TO 1/64
NEXT ASSY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL
CONTR NO
DR RD
12-80
CHK
11 FEB 81
APP'D
3-19-81
APPROVED
BY DIRECTION OF
tau-tron inc
DRAWING TITLE
MB 302
FRONT PANEL PC BOARD
SCHEMATIC
SIZE
D
CODE IDENT NO
DRAWING NO.
TDJ-54357
REV
C
SCALE 2
SHEET 2 OF 2


8
7
6
5
FRQ
GATE
COUNTER RESET
CLK IN
EXT.REF DATA
DATA IN
DATA IN
PHASE
0
1
2
3
+5V
1K
51
-2V
TP1
TP2
TP3
TP5
RPB-5
RPB-7
RPB-2
RPB-3
B1
10124
F4
1662
B5
1668F
RPS-7
C1
1678
D1
10125
VBB PIN(1)
470
5.2V
D
76"
A4
1688F
C6
A5
F100102
RG-178 20"
B5
F100131
SR.8"
C3
100
75
A7
1662
B7
B4
1688F
B6
10H116
A2
1692
C5
10212
51Ω
24"
SH.2 (D5-6,9 & E5-6,9)

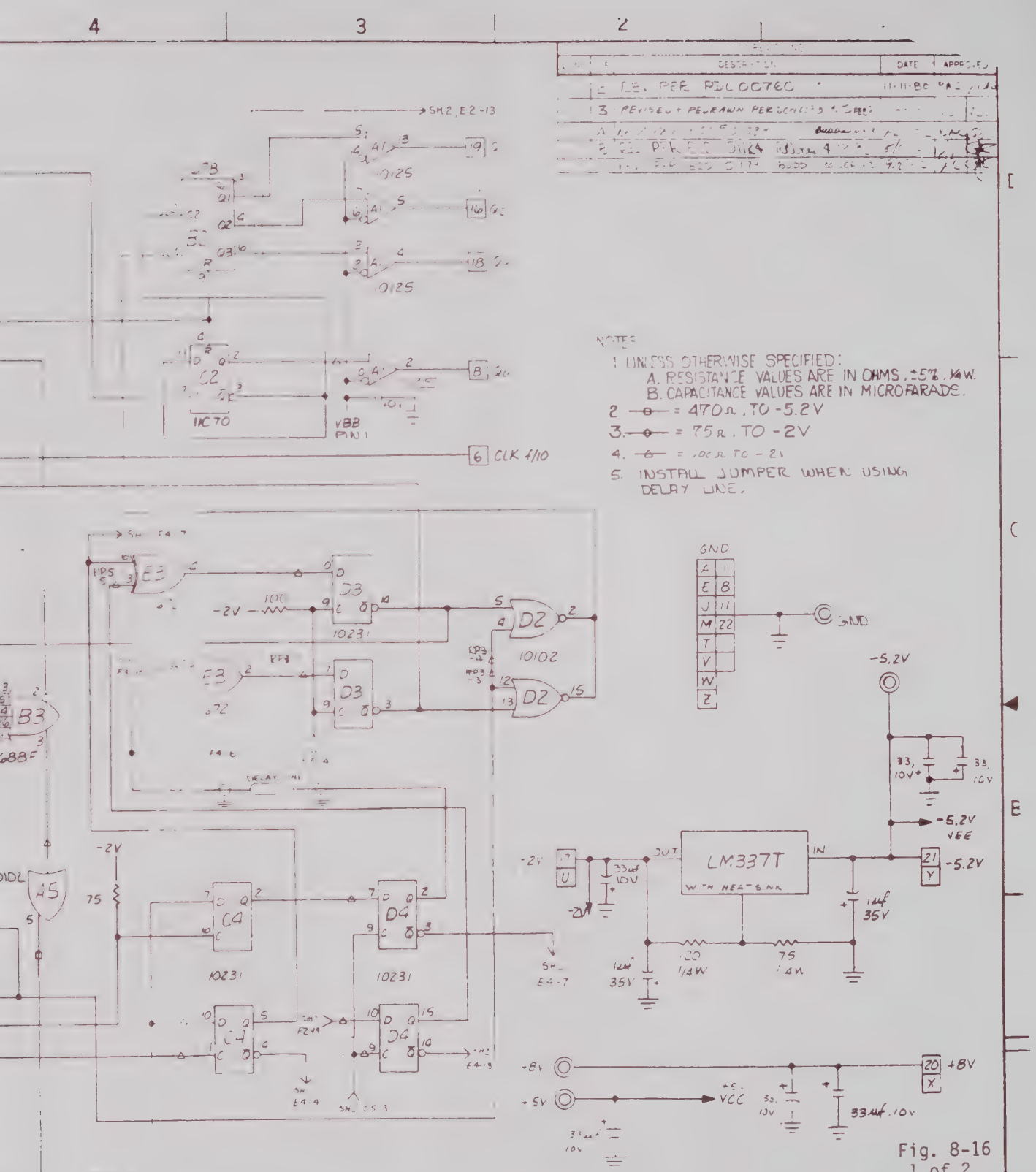
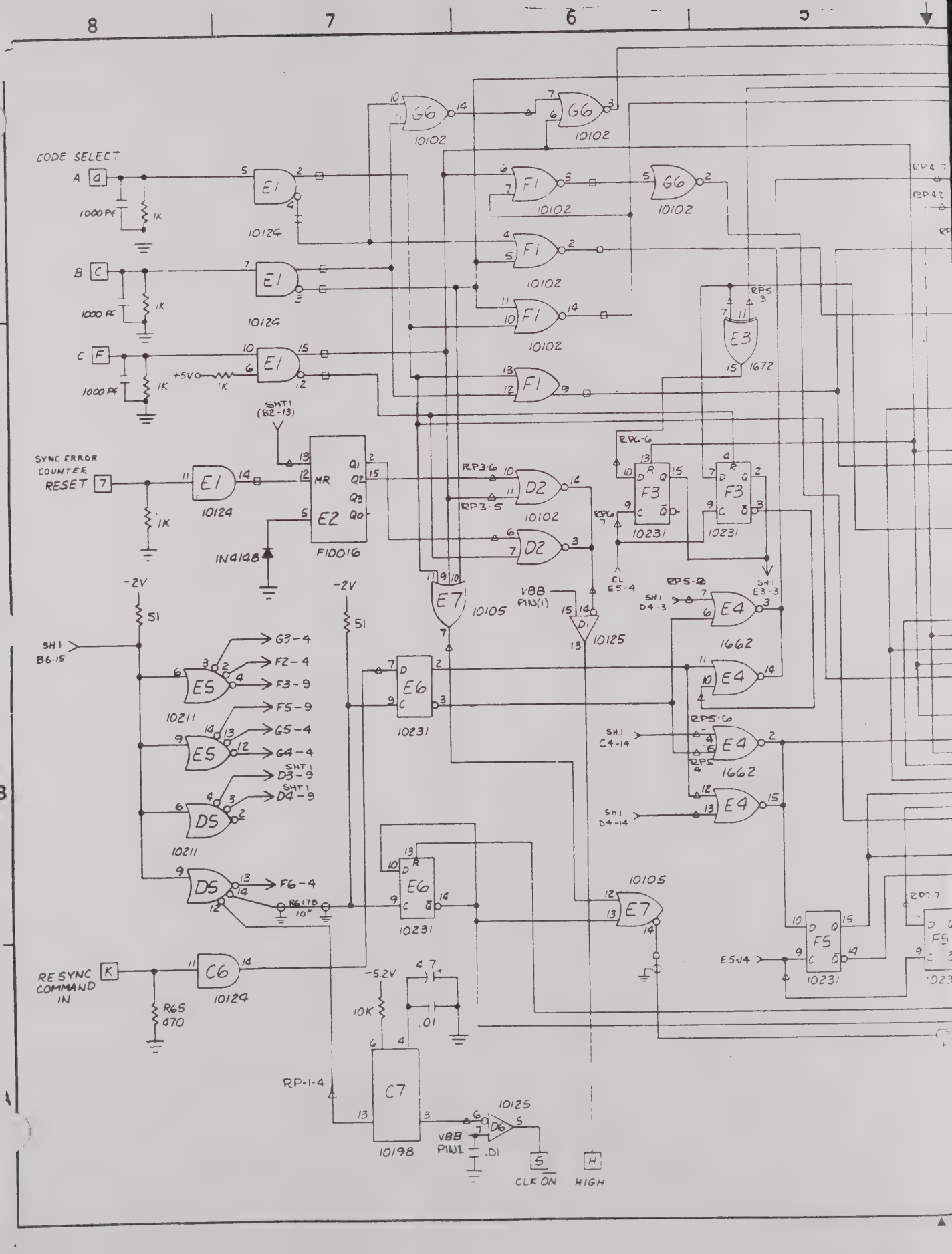


Fig. 8-16
1 of 2

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO	tau-tron inc
	TOLERANCES ANGLES ± —	DR R. DIONNE 12-80	DRAWING TITLE
	FRACTIONS ± —	CHK	MB 302 CODE RESYNC. SCHEMATIC DIAGRAM
	3 PLACE DECIMALS ± —	APPD	
	2 PLACE DECIMALS ± —		
	1 PLACE DECIMALS ± —		
NEXT ASSY / USED ON	MATERIAL	APPROVED	SIZE D / CODE IDENT NO. / DRAWING NO. TDU-54363 / REV
APPLICATION		BY DIRECTION OF	SCALE / SHEET 1 OF


8
7
6
CODE SELECT
A
B
C
1000 PF
1K
10124
SYNC ERROR COUNTER RESET
7
IN4148
F10016
SH1 (B2-13)
-2V
51
SH1 B6-15
G3-4
F2-4
F3-9
F5-9
G5-4
G4-4
SH1 D3-9
SH1 D4-9
10211
F6-4
RESYNC COMMAND IN
K
R65 470
C6
C7
10198
-5.2V
10K
.47
.01
RP-1-4
VBB PIN1
CLK ON
HIGH
G6
10102
F1
E1
E2
E3
1672
RP3-6
RP3-5
D2
F3
10231
CL E5-4
E7
10105
VBB PIN(1)
D1
10125
RP5-6
RP5-3
SH1 E3-3
SH1 D4-3
E4
1662
RP5-Q
RP5-6
SH1 C4-14
SH1 D4-14
E6
F5
E5J4
RP7-7

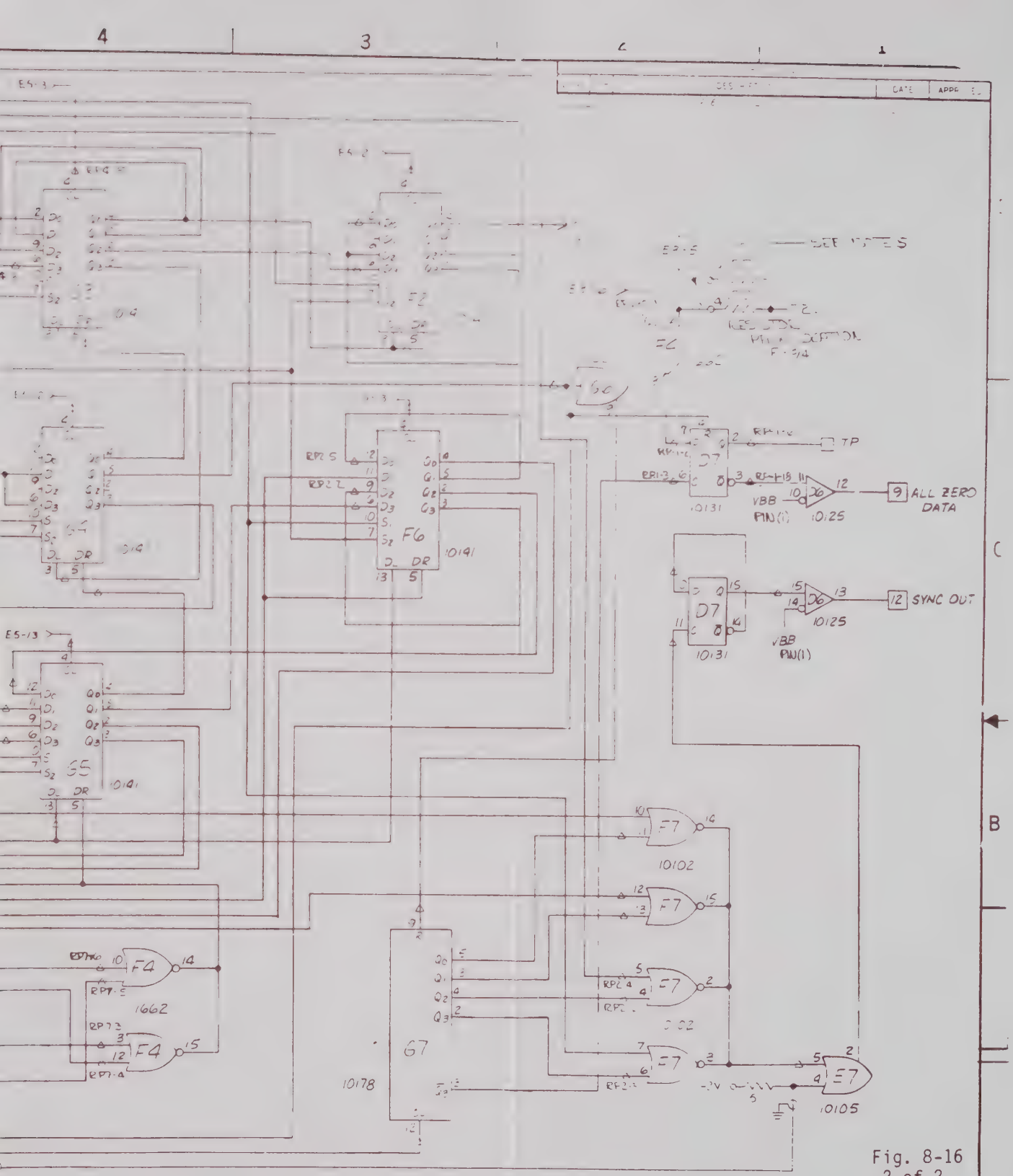
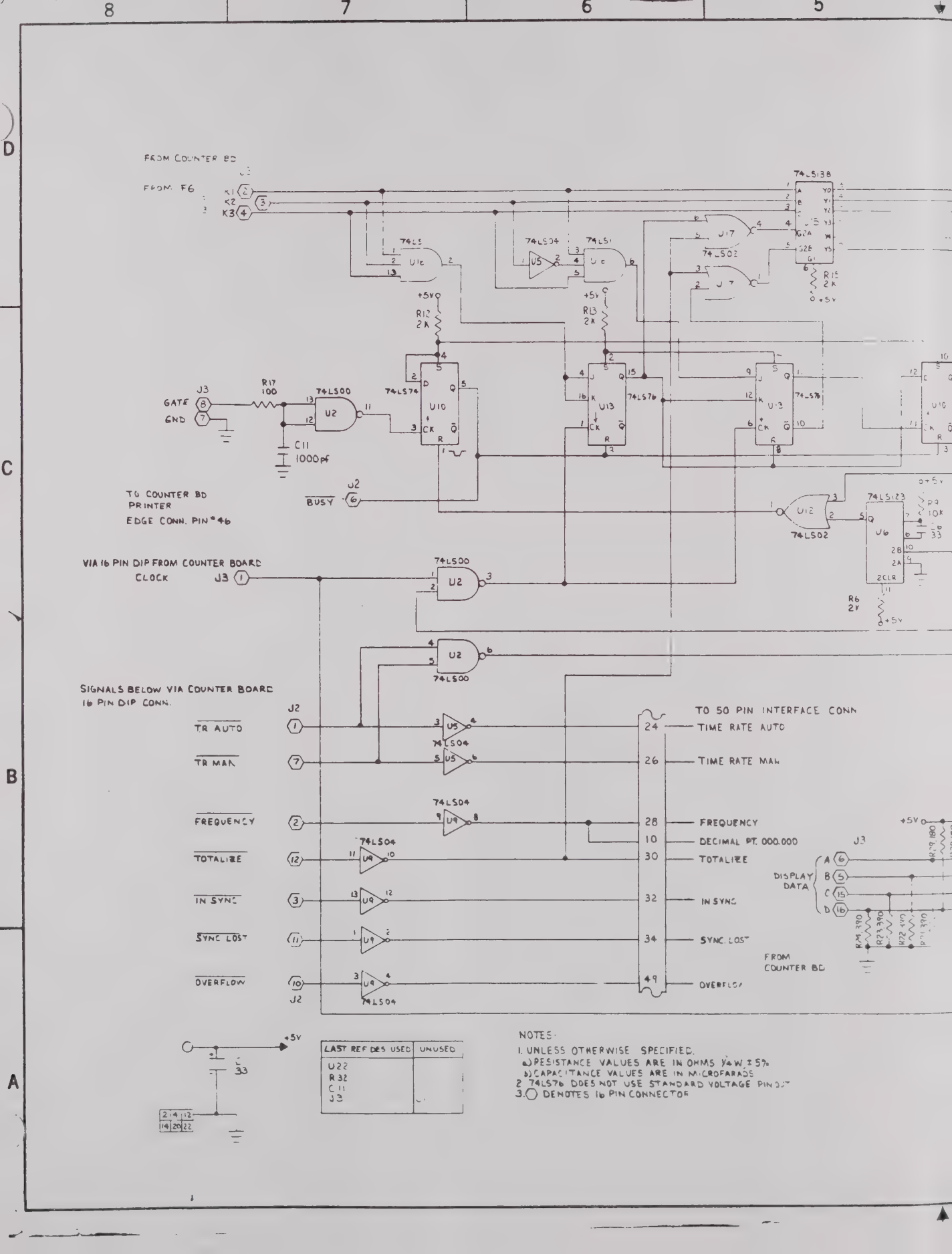
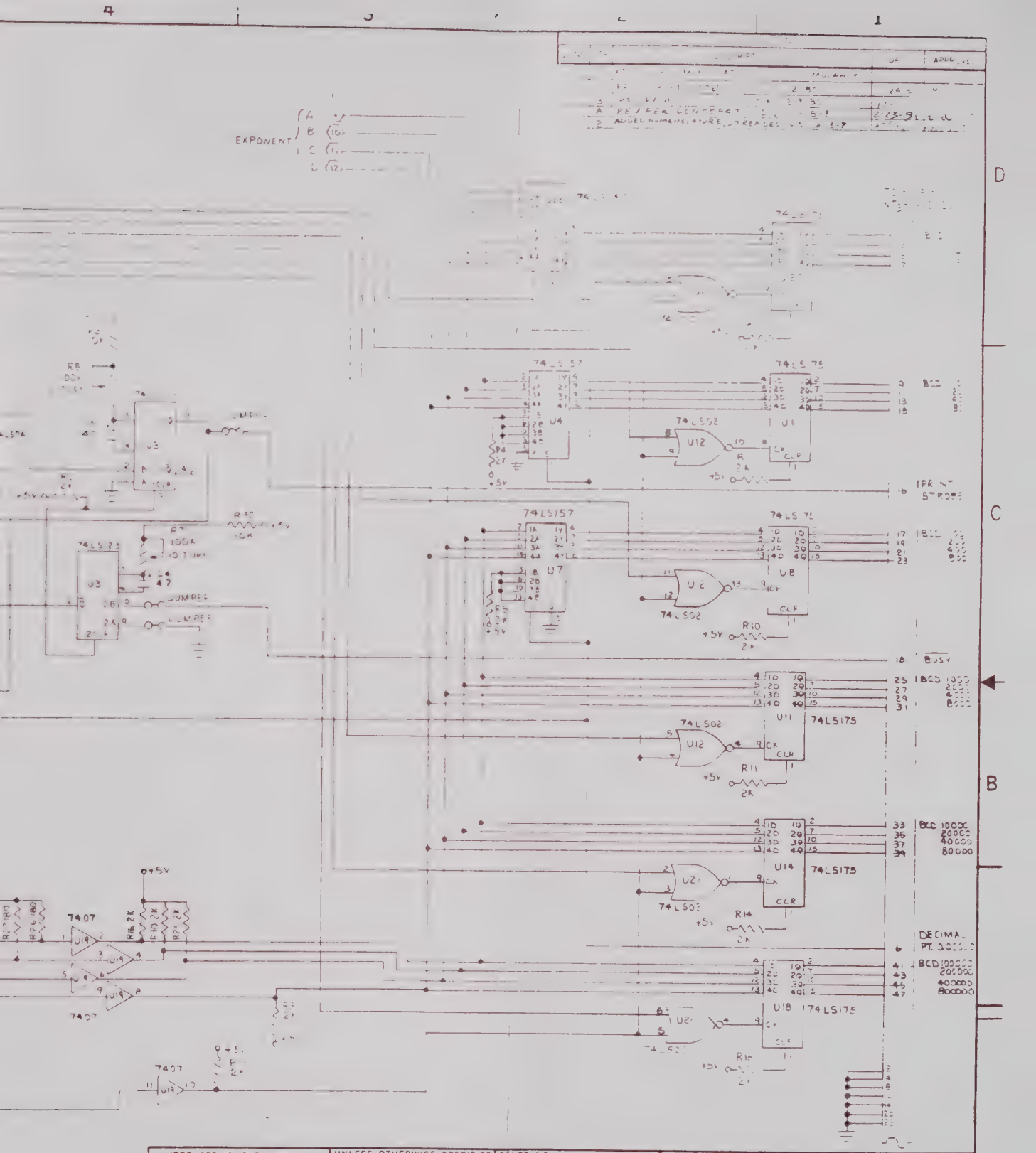


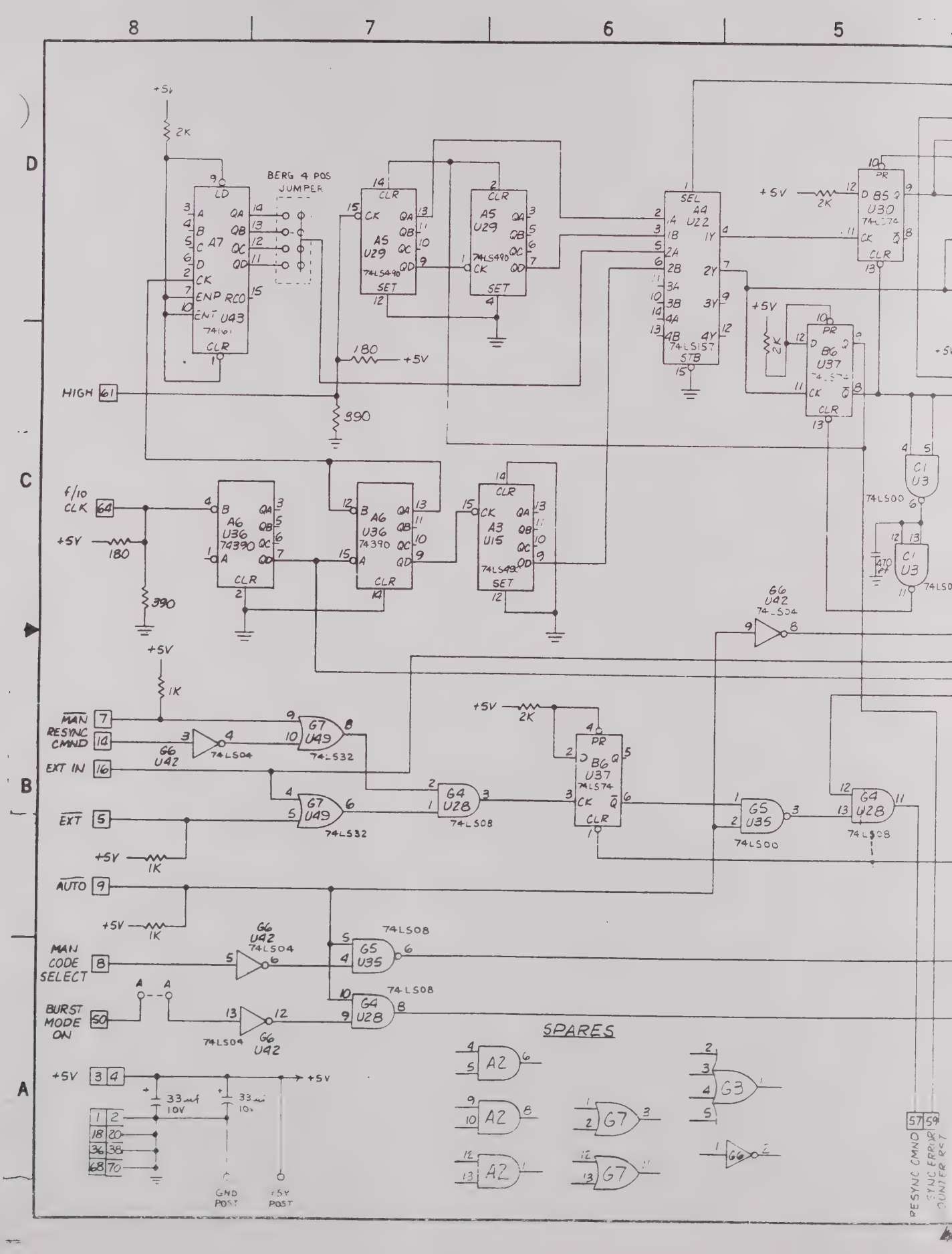
Fig. 8-16
2 of 2

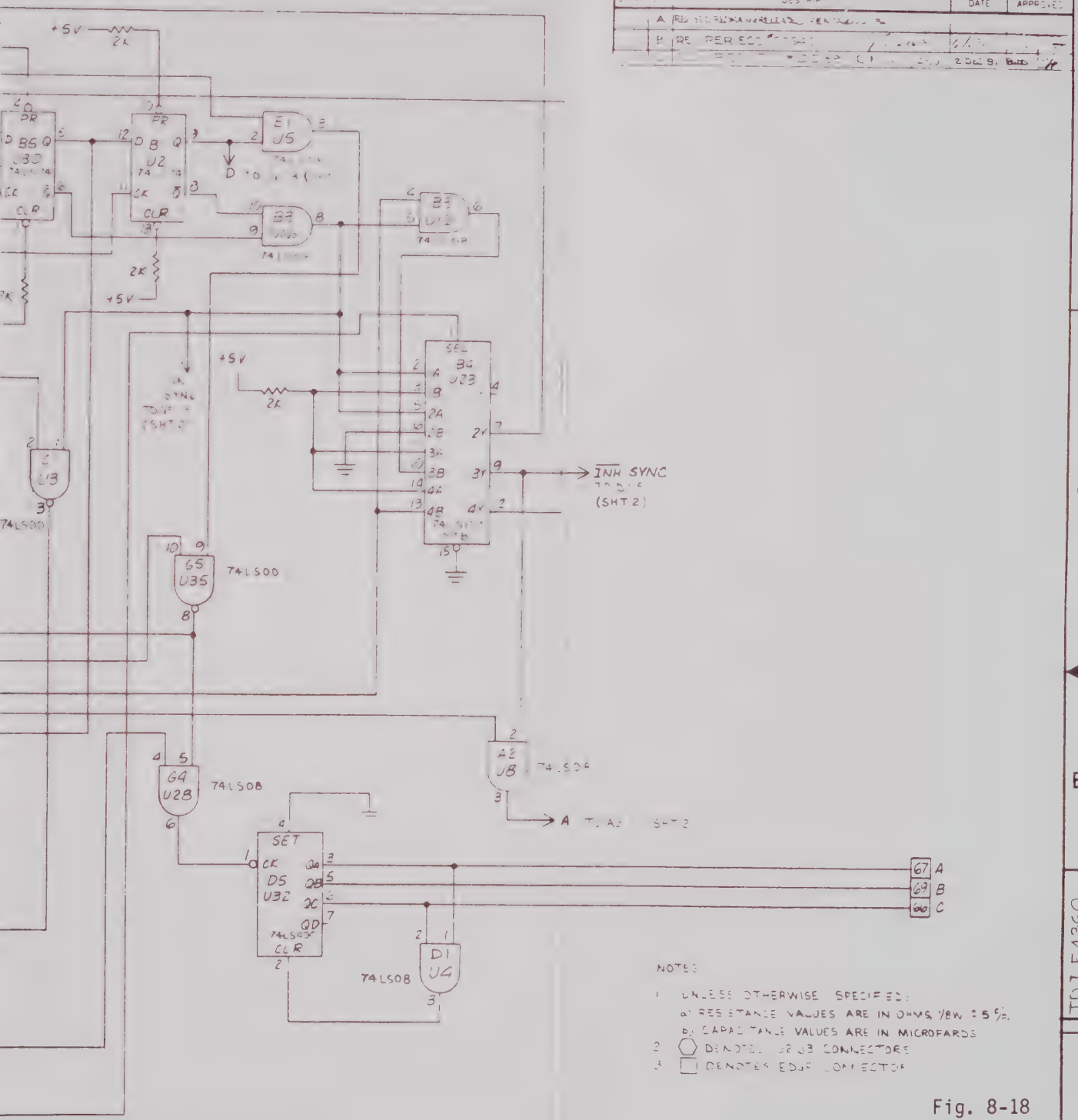
WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DRAWN CHK APPROVED BY DIRECTION OF	tau-tron INC DRAWING TITLE MB 302 CODE RESYNC. SCHEMATIC DIAGRAM
NEXT ASSY: TDJ-54364 MB302	USED ON		SIZE D · CODE IDENT NO · DRAWING NO TDJ-54363 · REV C
APPLICATION			SCALE — · SHEET 2


FROM COUNTER BD
FROM F6
K1
K2
K3
74LS138
74LS02
74LS04
74LS
+5V
R12 2K
R13 2K
R15 2K
J3
GATE
GND
R17 100
74LS00
U2
C11 1000pf
74LS74
U10
74LS76
U13
74LS73
U12
74LS123
U6
R6 2K
10K
.33
BUSY
TO COUNTER BD PRINTER EDGE CONN. PIN #46
VIA 16 PIN DIP FROM COUNTER BOARD
CLOCK
SIGNALS BELOW VIA COUNTER BOARD 16 PIN DIP CONN.
J2
TR AUTO
TR MAN
FREQUENCY
TOTALIZE
IN SYNC
SYNC LOST
OVERFLOW
TO 50 PIN INTERFACE CONN
24 TIME RATE AUTO
26 TIME RATE MAN
28 FREQUENCY
10 DECIMAL PT. 000.000
30 TOTALIZE
32 IN SYNC
34 SYNC. LOST
49 OVERFLOW
DISPLAY DATA
A
B
C
D
R20 180
R21 390
R22 390
R23 390
R24 390
FROM COUNTER BD
LAST REF DES USED
UNUSED
U22
R32
C11
J3
NOTES:
1. UNLESS OTHERWISE SPECIFIED.
a) RESISTANCE VALUES ARE IN OHMS ¼ W ± 5%
b) CAPACITANCE VALUES ARE IN MICROFARADS
2. 74LS76 DOES NOT USE STANDARD VOLTAGE PINOUT
3. ◯ DENOTES 16 PIN CONNECTOR



WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR C ATHERTON CHK APPD APPROVED BY DIRECTION OF	tau-tron inc DRAWING TITLE BCD INTERFACE SCHEMATIC Fig. 8-17 1 of 1
TDK-5443X / MB-302 NEXT ASSY / USED ON APPLICATION			SIZE C / CODE IDENT NO / DRAWING NO TDJ-3442B / REV C SCALE / SHEET


8
7
6
5
D
C
B
A
+5V
2K
BERG 4 POS JUMPER
LD
A7
ENP
ENT
U43
74161
RCO
CLR
A5
U29
74LS490
SET
180
HIGH 61
390
SEL
A4
U22
74LS157
STB
PR
B5
U30
74LS74
CK
D
Q
B6
U37
f/10 CLK 64
A6
U36
74390
A3
U15
C1
U3
74LS00
470pf
MAN RESYNC CMND 7
EXT IN 16
EXT 5
AUTO 9
MAN CODE SELECT 8
BURST MODE ON 50
1K
G7
U49
74LS32
G4
U28
74LS08
G5
U35
G6
U42
74LS04
A
33mf 10V
GND POST
+5V POST
SPARES
A2
G3
G7
RESYNC CMND 57
SYNC ERROR COUNTER RST 59

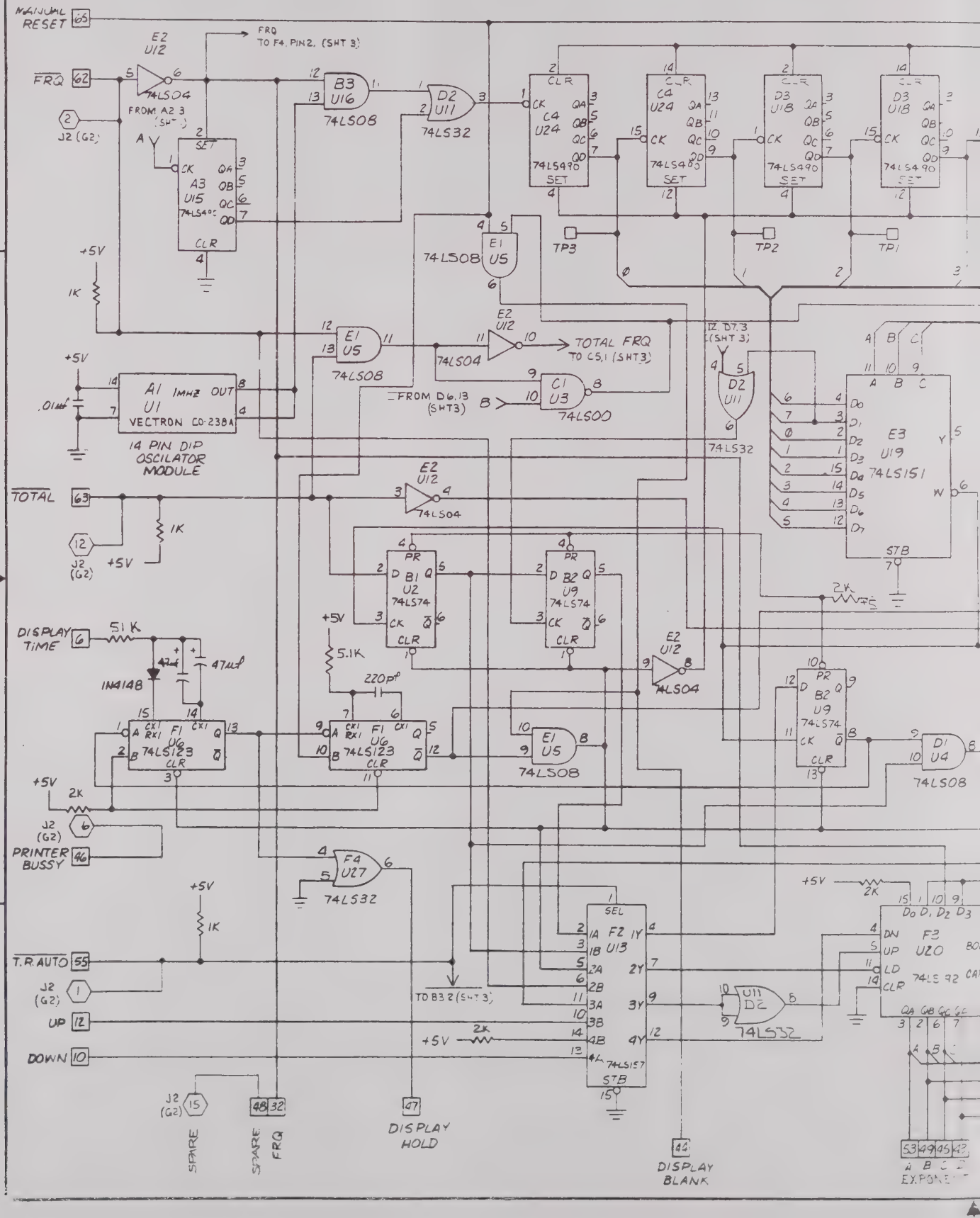


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE VALUES ARE IN OHMS, 1/8W ± 5%.
   b. CAPACITANCE VALUES ARE IN MICROFARDS
2. ⬡ DENOTES J2 OR J3 CONNECTORS
3. ▭ DENOTES EDGE CONNECTOR

Fig. 8-18
1 of 3

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTR NO	tau-tron inc
	TOLERANCES ANGLES ±	DR	
	FRACTIONS ±	CHK	
	3 PLACE DECIMALS ±	APPD	
	2 PLACE DECIMALS ±		DRAWING TITLE: MB302 COUNTER BD, SCHEMATIC DIAGRAM
	1 PLACE DECIMALS ±		
NEXT ASSY / USED ON	MATERIAL	APPROVED	SIZE D / CODE IDENT NO. / DRAWING NO. TDJ-54360 / REV C
APPLICATION		DO NOT SCALE DRAWING	SCALE — / SHEET 1 OF 3


MANUAL RESET 65
FRQ 62
J2 (G2) 2
E2 U12
74LS04
FROM A2.3 (SHT 3)
FRQ TO F4. PIN2. (SHT 3)
B3 U16
74LS08
D2 U11
74LS32
A3 U15 74LS490
CLR
+5V
1K
A1 1MHZ OUT U1 VECTRON CO-238A
14 PIN DIP OSCILATOR MODULE
.01uf
E1 U5
74LS08
TOTAL FRQ TO C5,1 (SHT3)
FROM D6,13 (SHT3)
C1 U3
74LS00
TOTAL 63
J2 (G2) 12
DISPLAY TIME 6
51K
47uf
IN4148
B1 U2 74LS74
B2 U9 74LS74
PR
CLR
5.1K
220pf
F1 U6 74LS123
2K
PRINTER BUSSY 46
F4 U27
74LS32
T.R.AUTO 55
J2 (G2) 1
UP 12
DOWN 10
TO B3.2 (SHT 3)
SEL
F2 U13
74LS157
STB
J2 (G2) 15
48 32
47
SPARE
SPARE
FRQ
DISPLAY HOLD
44
DISPLAY BLANK
IZ D7.3 (SHT 3)
D2 U11
74LS32
E3 U19 74LS151
TP3
TP2
TP1
F3 U20
74LS 92
DN
UP
LD
CLR
EXPONE

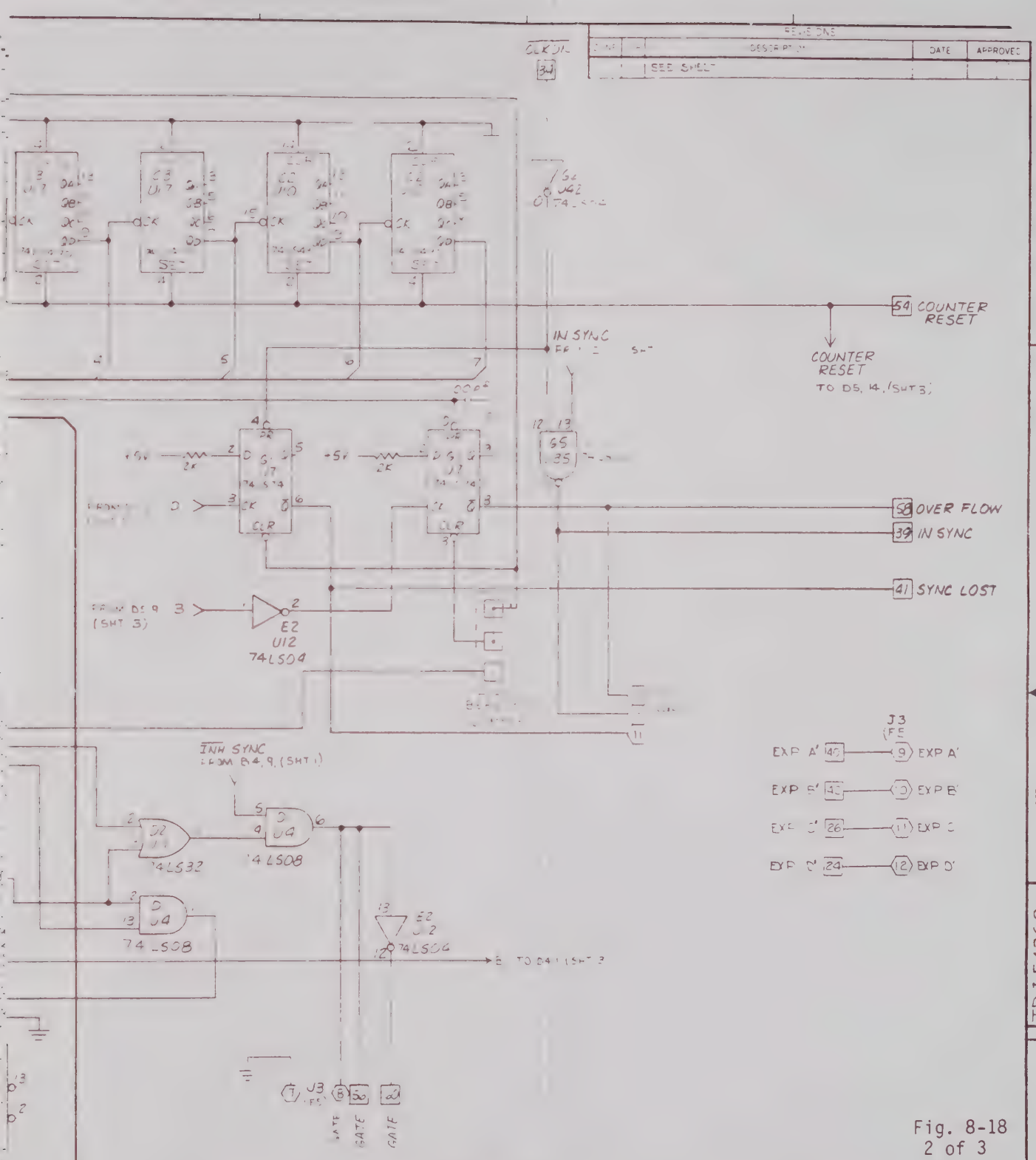
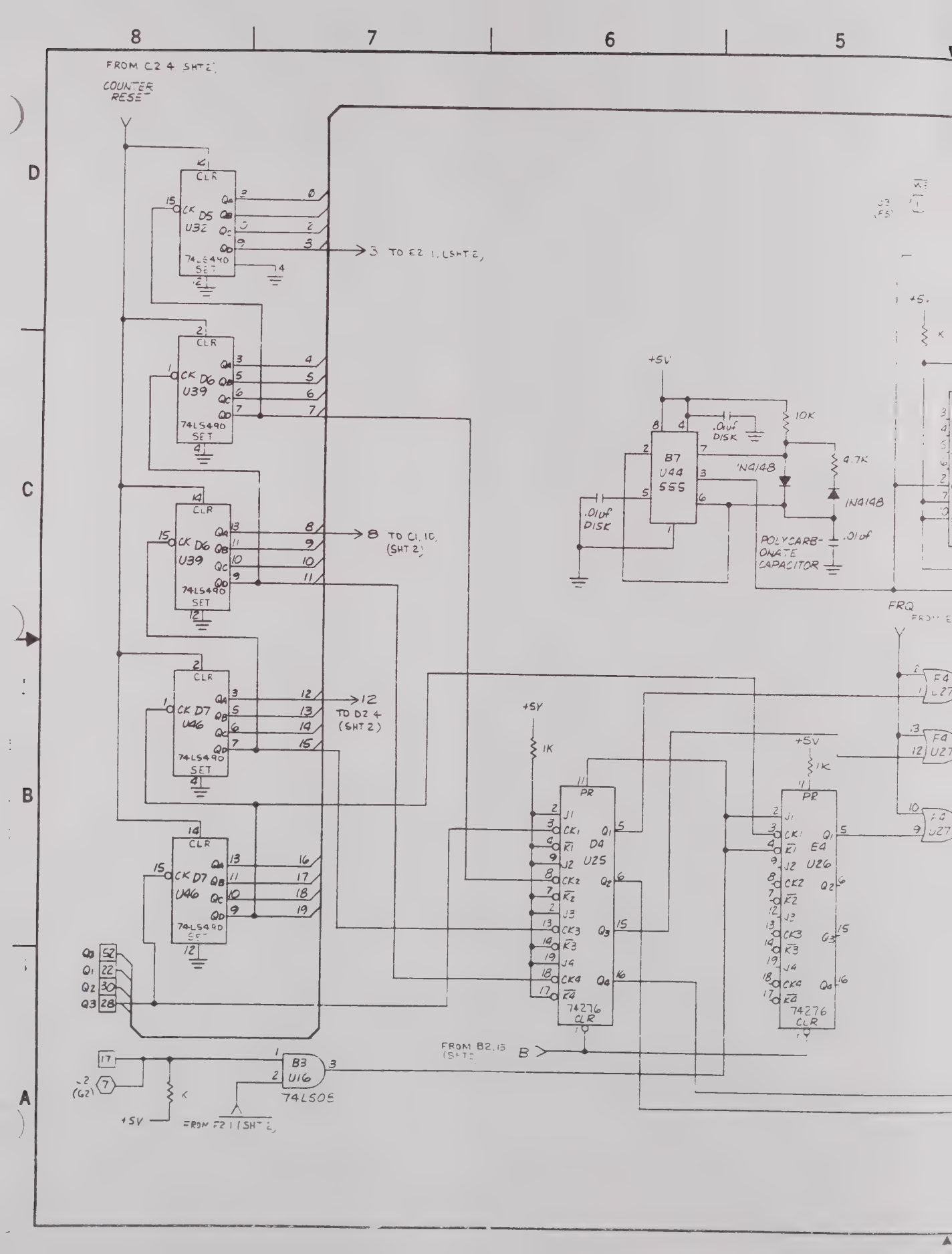


Fig. 8-18
2 of 3

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR RD 3-8-0 CHK APPD 7/1/	tau-tron inc DRAWING TITLE MB302 COUNTER BD. SCHEMATIC DIAGRAM
TOLERANCES NEXT ASSY / USED ON APPLICATION		APPROVED BY DIRECTION OF	SIZE D · CODE IDENT NO. · DRAWING NO. TDJ-54360 · REV C SCALE · SHEET 2 OF 3

TDJ-54360


8
7
6
5
D
C
B
A
FROM C2 4 SHT 2
COUNTER RESET
CLR
CK D5 U32
74LS490 SET
TO E2 1, (SHT 2)
CK D6 U39
TO C1, 10, (SHT 2)
CK D7 U46
TO D2 4 (SHT 2)
+5V
10K
.01uf DISK
B7 U44 555
1N4148
4.7K
POLYCARBONATE CAPACITOR
FRQ
1K
PR
J1
CK1
K1
J2
CK2
K2
J3
CK3
K3
J4
CK4
K4
74276 CLR
D4 U25
E4 U26
Q0
Q1
Q2
Q3
FROM B2.15 (SHT 2)
B
B3 U16
74LS05
FROM F2 11 (SHT 2)

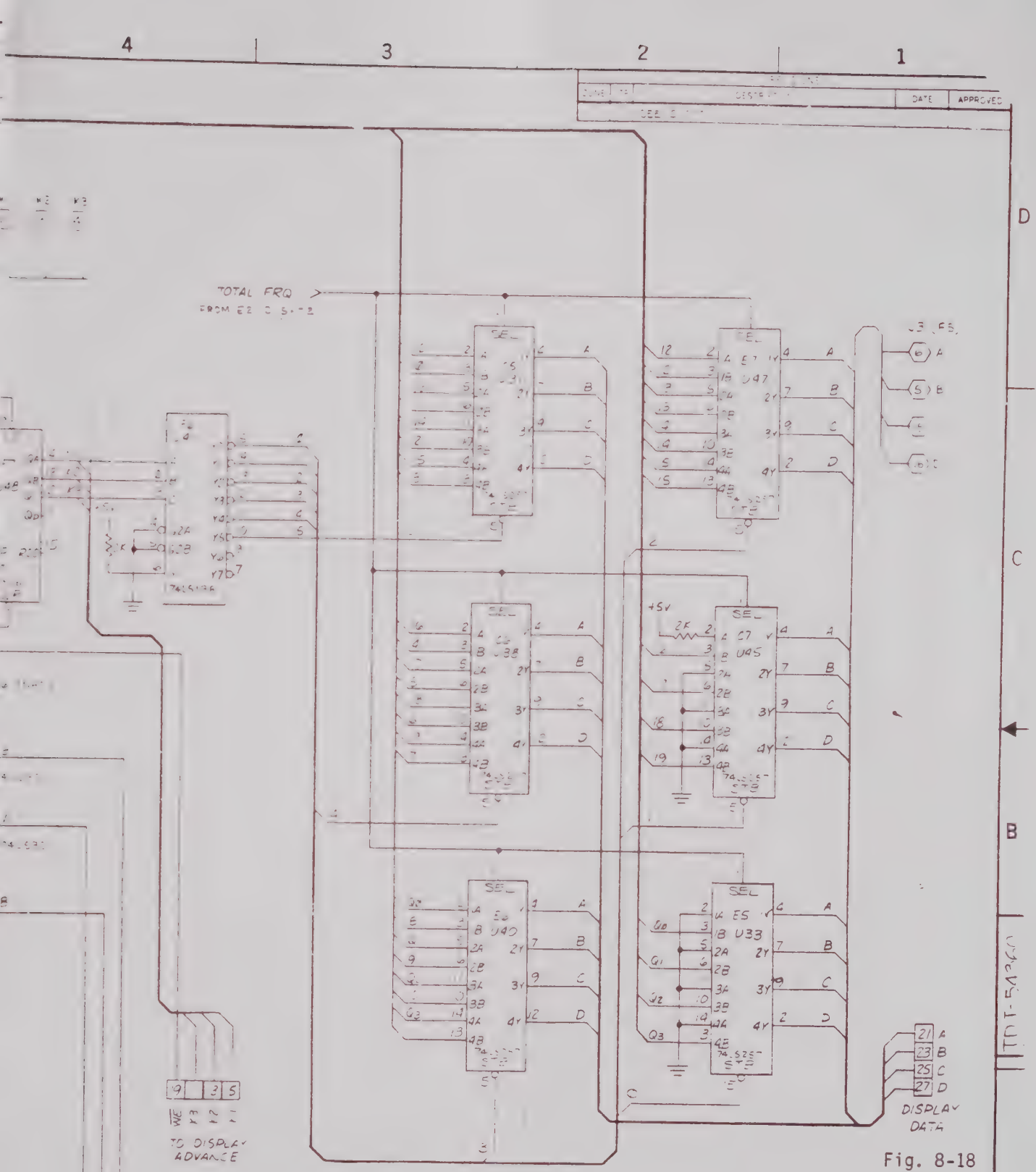
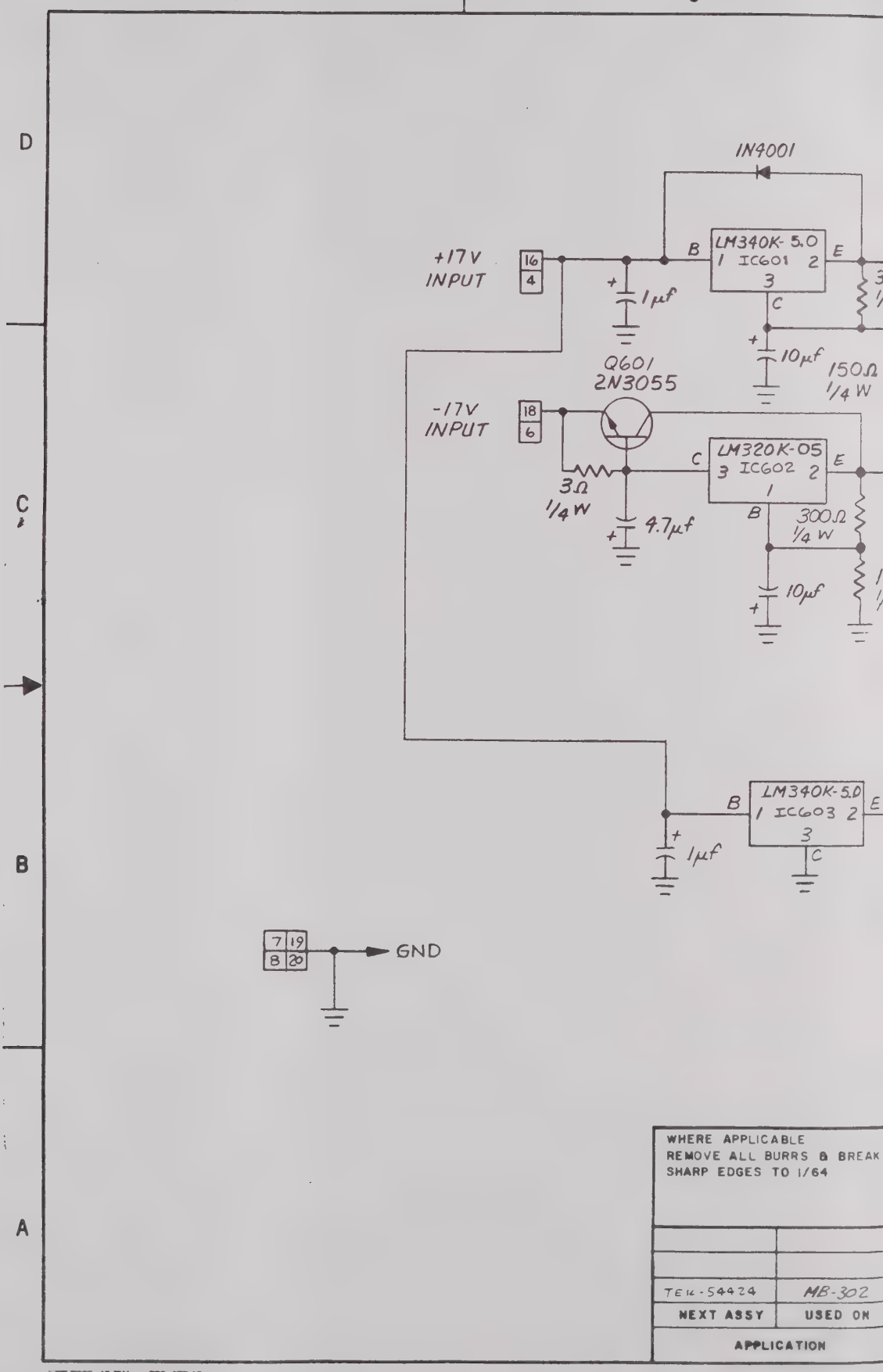


Fig. 8-18
3 of 3

WHERE APPLICABLE REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL	CONTR NO DR RD 2-80 CHK- 11 FEB 80 APPROVED 21 DIRECTION OF	tau-tron inc DRAWING TITLE MB302 COUNTER BD, SCHEMATIC DIAGRAM
TDM-54360-1			SIZE C · CODE IDENT NO · DRAWING NO TDM-54360 · REV C
NEXT ASSY	USED ON		SCALE · SHEET 3 OF 3
APPLICATION			


4
3
D
C
B
A
IN4001
+17V INPUT
16
4
LM340K-5.0
1 IC601 2
3
B
E
C
1μf
10μf
150Ω 1/4W
Q601 2N3055
-17V INPUT
18
6
LM320K-05
3 IC602 2
1
C
E
B
3Ω 1/4W
4.7μf
300Ω 1/4W
10μf
LM340K-5.0
1 IC603 2
3
B
E
C
1μf
7
19
8
20
GND
WHERE APPLICABLE
REMOVE ALL BURRS & BREAK
SHARP EDGES TO 1/64
TEK-54424
MB-302
NEXT ASSY
USED ON
APPLICATION

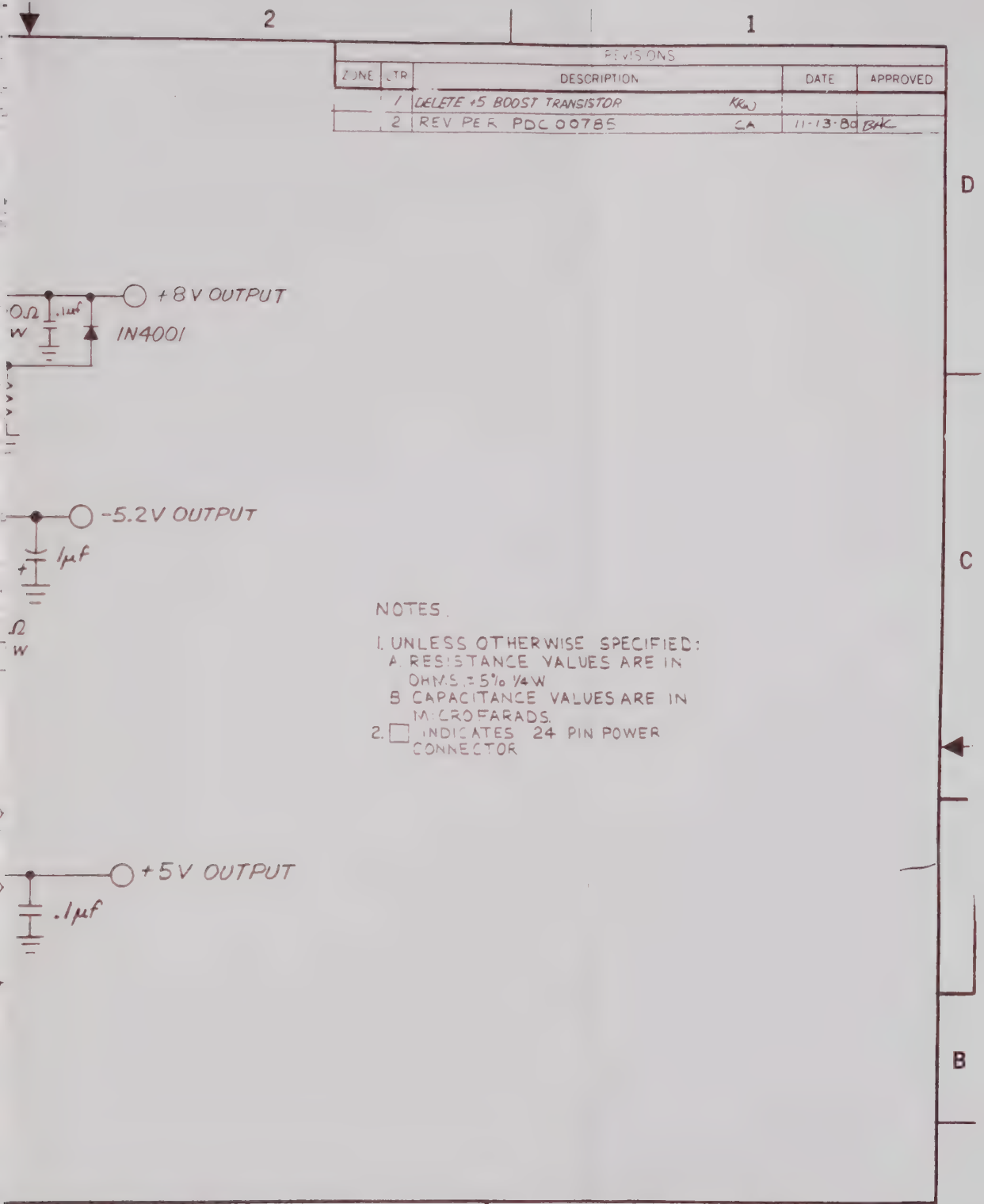
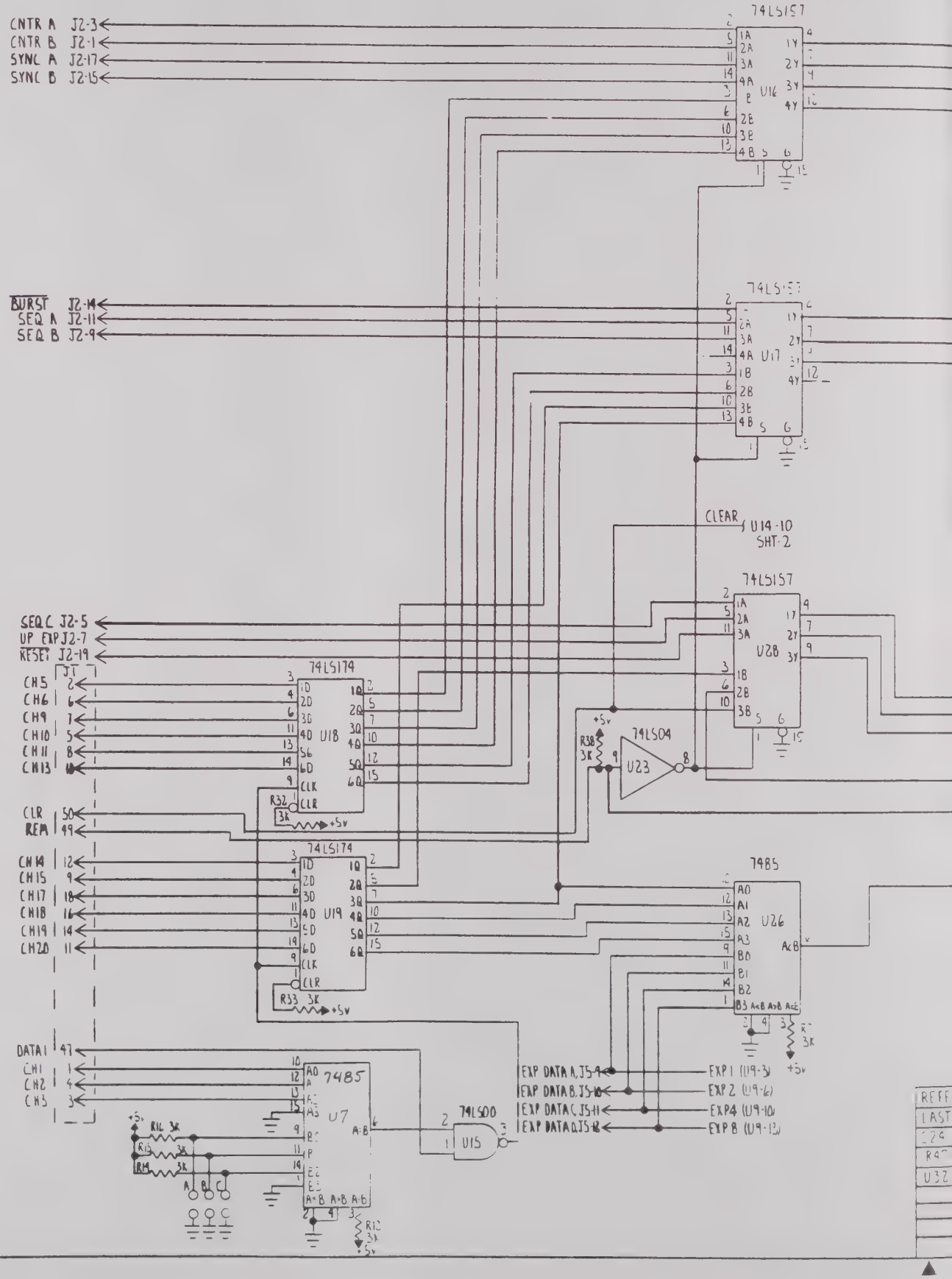

2
1
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
1 | DELETE +5 BOOST TRANSISTOR | KRW
2 | REV PER PDC 00785 | CA | 11-13-80 | BAK
D
+8V OUTPUT
Ω
W
.1mf
IN4001
-5.2V OUTPUT
1μf
Ω
W
NOTES.
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTANCE VALUES ARE IN OHMS, ±5% 1/4W
B CAPACITANCE VALUES ARE IN MICROFARADS.
2. ☐ INDICATES 24 PIN POWER CONNECTOR
C
+5V OUTPUT
.1μf
B
A
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± —
2 PLACE DECIMALS ± —
1 PLACE DECIMALS ± —
MATERIAL:
CONTR NO.
DR
CHK
APPD
APPROVED
BY DIRECTION OF
tau-tron inc
DRAWING TITLE
MB-302 POWER SUPPLY
SCHEMATIC +8V, +5V, -5V BOOST
SIZE C
CODE IDENT NO.
DRAWING NO. TCJ-54421
REV 2
SCALE NONE
TMI SERIES
SHEET 1 OF 1

Fig. 8-19
1 of 1

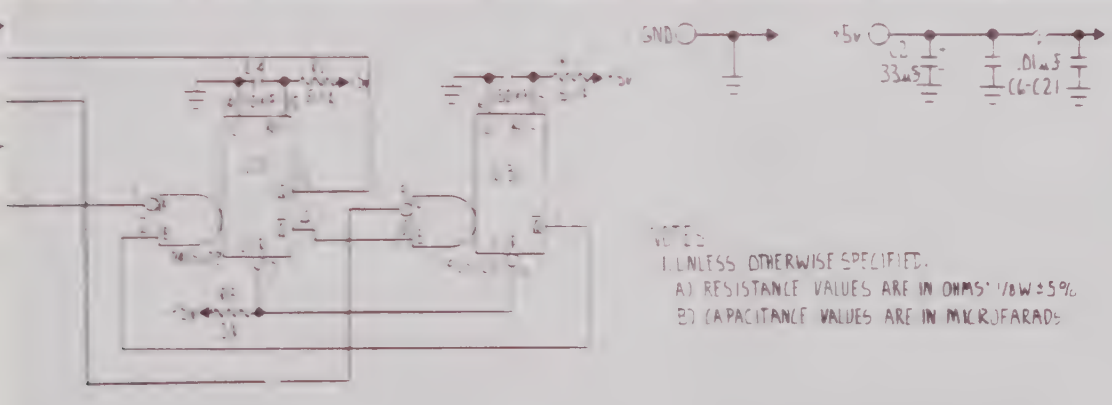

CNTR A J2-3
CNTR B J2-1
SYNC A J2-17
SYNC B J2-15
74LS157
U16
BURST J2-14
SEQ A J2-11
SEQ B J2-9
U17
CLEAR
U19-10
SHT-2
SEQ C J2-5
UP EXP J2-7
RESET J2-19
U28
CH5
CH6
CH9
CH10
CH11
CH13
74LS174
U18
R32
3K
+5v
74LS04
U23
R38
CLR
REM
CH14
CH15
CH17
CH18
CH19
CH20
U19
R33
7485
U26
DATA1
CH1
CH2
CH3
U7
R14
R13
R12
74LS00
U15
EXP DATA A J5-9
EXP DATA B J5-10
EXP DATA C J5-11
EXP DATA D J5-12
EXP 1 (U9-3)
EXP 2 (U9-6)
EXP 4 (U9-10)
EXP 8 (U9-12)

	A	REV PER ECO# 00993 JPP	17 JUN 81	6-18-81 RJL
	B	REV PER ECO#S1077 RN	2-23-82	3-4-82 BLDD RLC
	C	REDRAWN BMB	5-12-82	5-12-82

J2-4 CNTR A
J2-2 CNTR B
J2-18 SYNC A
J2-16 SYNC B

J2-13 $\overline{\text{BURST}}$
J2-12 SEQ A
J2-10 SEQ B

J2-6 SEQ C
J2-8 UP FRQ
J2-20 $\overline{\text{RESET}}$



NOTES
1. UNLESS OTHERWISE SPECIFIED.
   A) RESISTANCE VALUES ARE IN OHMS' 1/8W ±5%
   B) CAPACITANCE VALUES ARE IN MICROFARADS

Fig. 8-20
1 of 2

USED	UNUSED		
	R13		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

CONTR NO
DRDA PERLMUTTER 12/9/81
CHK J COOPER 12/15/81
APPR J PERLMUTTER

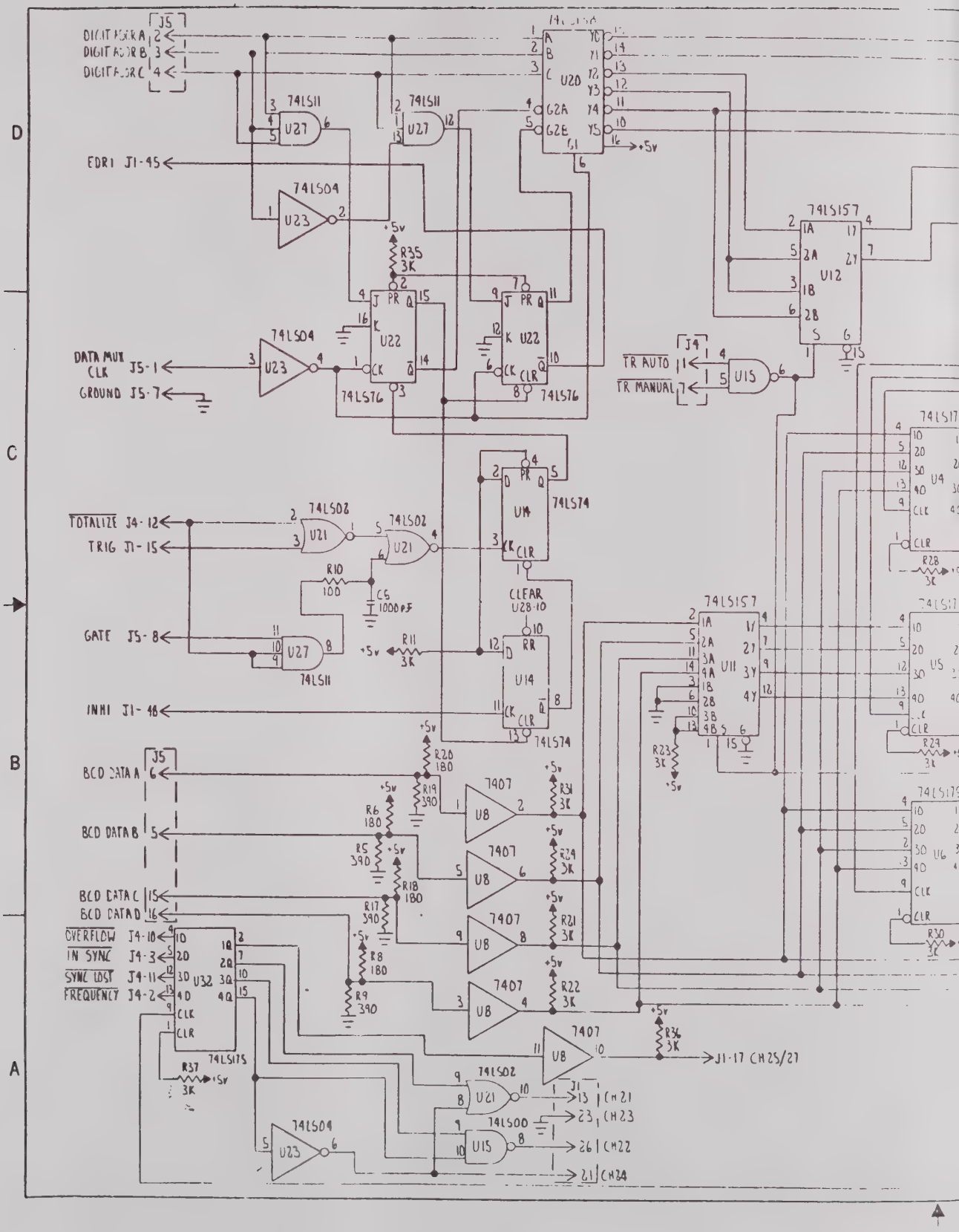
tau-tron inc

DRAWING TITLE
SCHEMATIC
MB-302
TM1 MODULE GPIB ADAPTOR

D-54543	MB-302	D	D-54542
NEXT ASSY	USED ON	TM1 EPIE	SHEET 1 OF

APPLICATION

D 54542


J5
DIGIT ADDR A
DIGIT ADDR B
DIGIT ADDR C
74LS11
U27
EDR1 J1-45
74LS04
U23
+5v
R35 3K
74LS74
U22
DATA MUX CLK J5-1
GROUND J5-7
74LS76
74LS157
U12
J4
TR AUTO
TR MANUAL
U15
TOTALIZE J4-12
TRIG J1-15
74LS02
U21
R10 100
C6 1000pF
CLEAR U28-10
U14
GATE J5-8
R11 3K
INH1 J1-46
U11
R23 3K
R28 3K
R29 3K
R30 3K
BCD DATA A
BCD DATA B
BCD DATA C
BCD DATA D
7407
U8
R6 180
R5 390
R18 180
R17 390
R8 180
R9 390
R19 390
R20 180
R31 3K
R24 3K
R21 3K
R22 3K
R36 3K
OVERFLOW J4-10
IN SYNC J4-3
SYNC LOST J4-11
FREQUENCY J4-2
U32
74LS175
R37 3K
J1-17 CH25/27
J1-13 CH21
J1-23 CH23
J1-26 CH22
J1-21 CH24
74LS00
U4
U5
U6

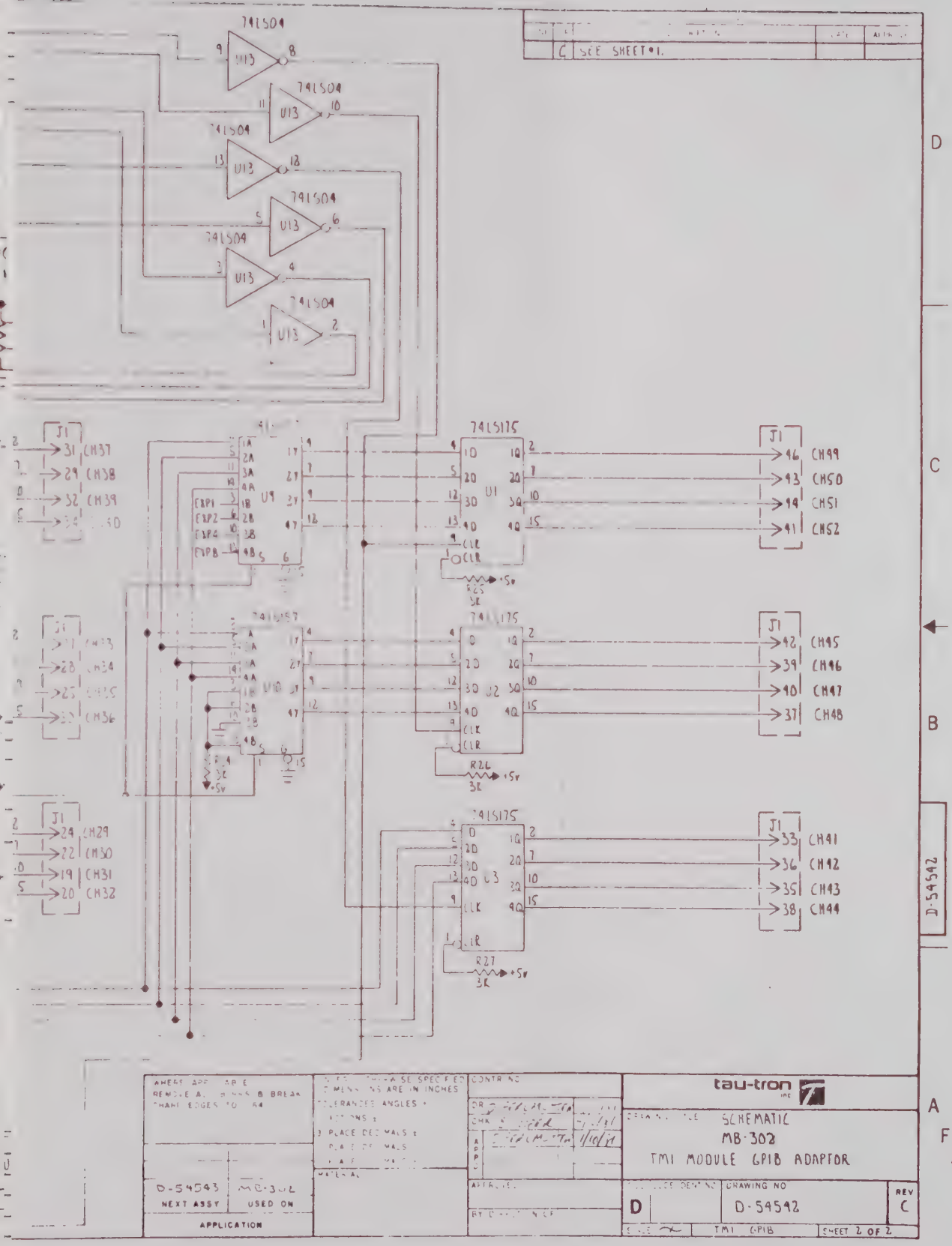

74LS04
U13
74LS175
U1
U2
U3
U9
U10
J1
CH37
CH38
CH39
CH40
CH33
CH34
CH35
CH36
CH29
CH30
CH31
CH32
CH49
CH50
CH51
CH52
CH45
CH46
CH47
CH48
CH41
CH42
CH43
CH44
R25
R26
R27
3K
+5V
SCE SHEET #1.
tau-tron
SCHEMATIC
MB-302
TMI MODULE GPIB ADAPTOR
D-54542
D-54543
NEXT ASSY
MB-302
USED ON
APPLICATION
DRAWING NO
REV
C
SHEET 2 OF 2

Fig. 8-20
2 of 2

APPENDIX A

Version 4 IFC

This appendix is intended to acquaint the user with the Software Version 4 MF-5 Interface card as implemented in the BERTS-325C/650 Bit Error Measurement System. The information contained in this appendix assumes that the user is familiar with the GPIB operating procedures as described in Sections 3, 4, 5 and 6. These procedures describe in detail how to operate the BERTS-325C/650 Bit Error Measurement System in the GPIB mode.

The software changes incorporated are:

1. The polarity of seven of the eight address inputs has been reversed. The SRQ Enable has not been changed. As a result, the orientation of the rear-panel GPIB Dip switch has been reversed; only the nomenclature of the SRQEN switch has been externally changed.
2. An IFC instruction no longer clears the entire card, only the Bus interface.
3. The user no longer has to implement two Bus Input instructions consecutively to read data from the MB-302. It is only necessary to do a DCL (device clear), then a single Bus Input to receive current data. This eliminates the need for double transfers of data.

As a result of these changes, the BERTS-325C/650 GPIB performs more closely to IEEE-488-1978 (GPIB) standards and makes it easier for the user to implement. This new software became effective with serial number 8301001. The manual has been revised to reflect both software versions.

APPENDIX B

BERTS-325C/650 GPIB
and
Ready Reference Guide

INTRODUCTION

This appendix contains a brief summary of the BERTS-325C/650 system GPIB operation. The information contained in the summary assumes that the user is familiar with IEEE-488-1978 (GPIB) standards. However, if the user is not familiar with these standards, he should refer to the manual under Sections 3, 4, 5 and 6 for GPIB operation. A ready reference guide (presented in tabular format) is also included in this appendix. The guide describes each module GPIB message format, measurement output, and mode of operation.

BERTS-325C/650 GPIB OPERATION

The BERTS-325C/650 system GPIB operation has been designed similar to many other GPIB systems that utilize compatible instruments. That is, flexibility offered in the BERTS-325C/650 GPIB allows for an easily configured system tailored to specific application requirements. This type of system (BERTS-325C/650) controls the data and transmits them between the modules (except for the ME-302) within the system. To understand a little more about the BERTS-325C/650 GPIB, a brief description of the characteristics of the MF-5 and the modules is presented in the following paragraphs.

MF-5 MAINFRAME

The GPIB hardware interface contained in the MF-5 Mainframe provides the boundary where all the modules (except for the ME-302) are connected in the BERTS-325C/650 system. The front and rear panels of the MF-5 allow for ease of indication and access to the system's GPIB operation, respectively. For additional details regarding the use of the MF-5 Mainframe GPIB operation, refer to Section 6, GPIB OPERATION, in the manual.

BERTS-325C/650 MODULES

To interface with the MF-5 Mainframe, each module (except the ME-302) is provided with a GPIB personality card. This card permits each module uninterrupted connection to the MF-5 Mainframe. Whenever a measurement is available, the GPIB will access it. Thus, the user is always assured of a measurement whenever he needs it. Additionally, the following benefits are available:

1. Greater measurement speed.
2. More accurate results.
3. Reduced random errors caused by operator fatigue.
4. Reduced manual handling of data because data are automatically entered vice manually entered.

For further details, refer to Sections 3, 4, and 5, GPIB OPTION.

NOTE: It is recommended practice that the user become familiar with the GPIB operation of the BERTS-325C/650 system; otherwise the system will not perform properly nor will it perform to the user's requirements.

READY REFERENCE GUIDE

This section contains a ready reference guide (in tabular format) of the MS, MN, and MB-302 modules. This guide is primarily aimed at users already familiar with IEEE-488-1978 (GPIB) standard operations. For further details, refer to the individual module sections (3, 4, and 5) in the manual.

NOTE: The ready reference guide should only be used for quick reference to the module modes of operation, GPIB message formats and their measurement outputs.

MS-302 GPIB OPERATION

General

All front-panel controls, except the VCO VERNIER, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An associated Address/ Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired

Message Format

The message consists of four digits (in ASCII code) followed by a terminator.

Ident	VCO/ CRYSTAL	CRYSTAL/ VCO RANGE	CRYSTAL OSC SELECT	Termi- nator

Ident

Digit	Meaning
1	MS-302 Clock Source

VCO/CRYSTAL

Digit	Meaning
0	CRYSTAL
1	VCO

CRYSTAL/ VCO RANGE

Digit	Meaning
0	175 to 325MHz; or full crystal frequency
1	100 to 175MHz; or crystal ÷10
2	10 to 100MHz; or crystal ÷100
3	1 to 10MHz; or crystal ÷1000
4	0.1 to 1MHz; or crystal ÷10000
5	10 to 100kHz; no output in crystal mode
6	1 to 10kHz; no output in crystal mode
7	Illegal (no output)

CRYSTAL/ OSC SELECT

Digit	Meaning
0	1st crystal frequency
1	2nd crystal frequency
2	3rd crystal frequency
3	Illegal (no output)

Terminator

Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

MN-302 GPIB OPERATION

General

All front-panel controls, except the Clock INPUT slide switch, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An asscociated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired.

Message Format

The message consists of five digits (in ASCII code) followed by a terminator.

Ident	ERR INJ	PATTERN	RZ/NRZ DATA	D/$\overline{D}$ DLY DATA	Termi-nator

Ident

Digit	Meaning
2	MN-302

ERR INJ

Digit	Meaning
0	OFF
1	Internal Error Injection
2	External Error Injection
3	Illegal

PATTERN

Digit	Meaning
0	2^7-1 pseudorandom pattern
1	2^{15}-1 pseudorandom pattern
2	2^{20}-1 pseudorandom pattern
3	2^{23}-1 pseudorandom pattern
4	16-bit pattern A
5	16-bit pattern B
6	16-bit pattern C
7	16-bit pattern D

RZ/NRZ DATA

Digit	Meaning
0	RZ DATA
1	NRZ DATA

D/$\overline{D}$ DELAYED DATA

Digit	Meaning
0	$\overline{D}$ DELAYED DATA
1	D DELAYED DATA

TERMINATOR

Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

MB-302 GPIB OPERATION

GENERAL

All front-panel controls, except CLOCK/DATA INPUTS PHASE and MANUAL SYNC switches, can be remotely controlled by a GPIB-compatible controller. The controller connects to the rear panel of the MF-5 Mainframe. An associated Address/Control switch, also on the rear panel of the MF-5, must be properly set for the type of operation desired. This option replaces the standard printer output.

MESSAGE Format

The message consists of five digits (in ASCII code) followed by a terminator.

Ident	CNTR Mode	SYNC Mode	REF DATA	BER EXP	Termi-nator

Ident

Digit	Meaning
3	MB-302

CNTR Mode

Digit	Meaning
0	Bit error rate-Manual range
1	Bit error rate-Auto range
2	TOTALIZE
3	Clock frequency

SYNC Mode

Digit	Meaning	
0	Auto synchronization	
1	Manual synchronization	Burst
2	EXT COMMAND sync	mode
3	EXT REF DATA	enabled
4	Auto synchronization	
5	Manual synchronization	Burst
6	EXT COMMAND sync	mode
7	EXT REF DATA	disabled

Internal REF DATA

Digit	Meaning
0	2^7-1 pseudorandom pattern
1	2^{15}-1 pseudorandom pattern
2	2^{20}-1 pseudorandom pattern
3	2^{23}-1 pseudorandom pattern

Digit	Meaning
4	Any 16-bit pattern
5	Illegal
6	Illegal
7	Illegal

BER Exponent — Any number in ASCII code between 2 and 9 inclusive.

Terminator — Terminators recognized are Comma, CR and LF. Alternatively, an EOI signal may be used as the message terminator.

Measurement Output — Place the MF-5 in TALK mode following GPIB protocol. The MF-5 will now send measurement and status data back to the GPIB controller when available. No prior module ID setup is necessary since the MF-5 interface will support only one GPIB talker module. Whenever a measurement is available, the MB-302 will load the measurement value and status bits into the MF-5 GPIB interface. If addressed to talk, the MF-5 GPIB interface will immediately send an 11-character (ASCII code) message containing a space between the status digit and measurement (including overflow) digits, followed by the terminators CR and LF.

STATUS DIGIT	SPACE	OVER-FLOW DIGIT	MSD	2nd	3rd	4th	5th	LSD	CR	LF

Definition of the digits are as follows:

STATUS DIGIT:

ASCII DIGIT	SYNC LOST	IN SYNC
0	FALSE	FALSE
1	FALSE	TRUE
2	TRUE	FALSE
3	TRUE	TRUE
+	FREQUENCY MEASUREMENT	
OTHER VALUES	ILLEGAL	

OVERFLOW DIGIT:

+	OVERFLOW TRUE
SPACE	OVERFLOW FALSE

MSD THRU LSD:

Decimal numbers, period, or minus sign

MEASUREMENT	FORMAT (MSD FIRST)
BIT ERROR RATE	A . BC - D
TOTALIZE	A B C D E F
FREQUENCY	A B C D E F (in kHz)

Measurements become available at the end of the measurement gating period. This happens automatically in all counter modes except TOTALIZE. For a TOTALIZE measurement, the gating period is infinite; thus, the MB-302 will not automatically generate a measurement output. The controller can request the current total error measurement by issuing a group execute trigger (GET) while the MF-5 is addressed to LISTEN. A service request will be generated if enabled.

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Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

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Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

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